

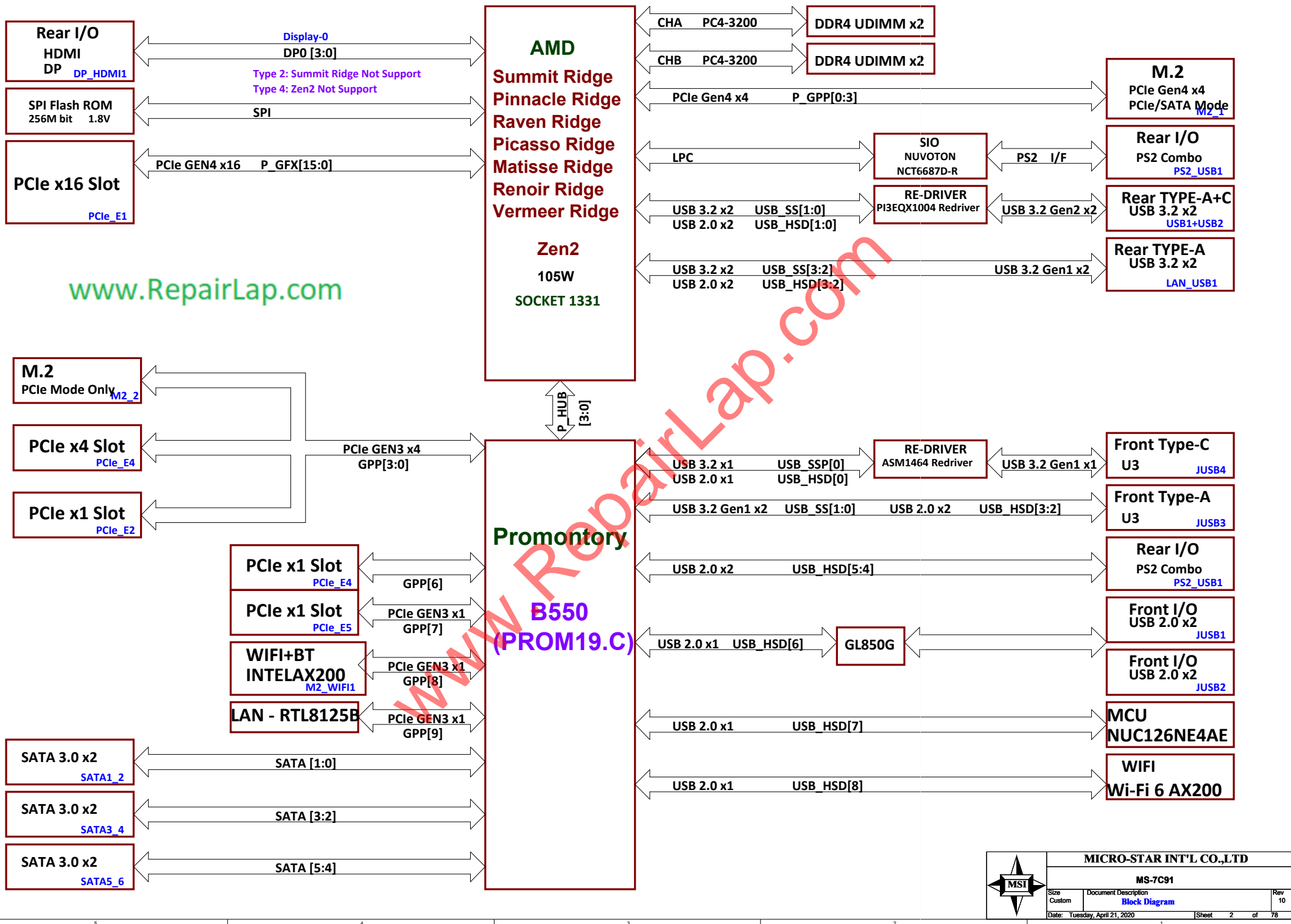
AMD AM4 B550

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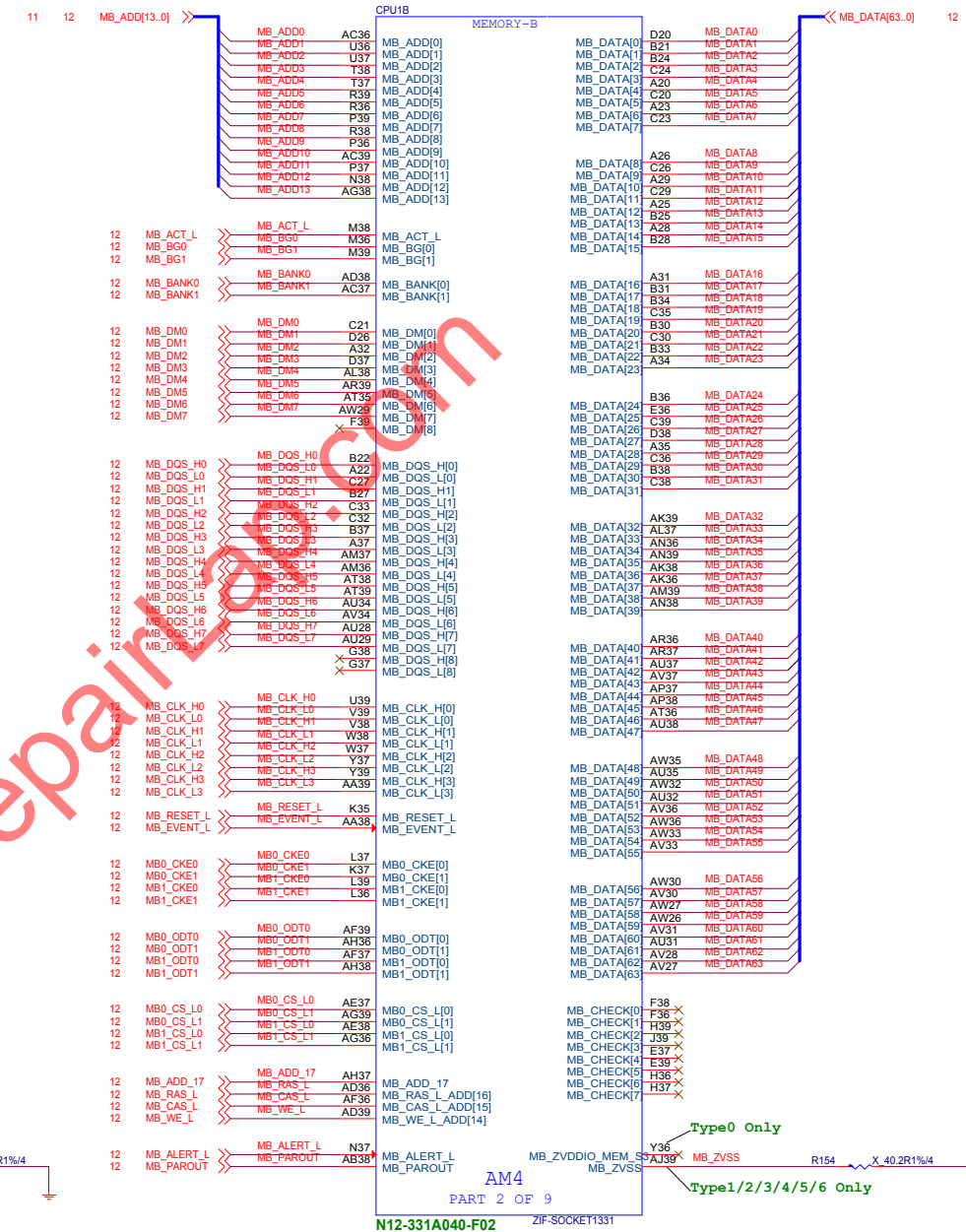
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25	M2_2 PCIE Only(KEY_M)	56	CPU power VDDP - NB503		
26	M2_WiFi1(KEY_E)	57	VRM PWRGD		
27	SIO NCT6687D-R	58	DDR Power - RT8125H		
28	SIO HW Monitor	59	DDR PWR-MP2329G-VPP25 / VTT		
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31	FAN TYPE-M SYSFAN1/2	62	OV Control - NCT3933		
32	FAN TYPE-M SYSFAN3/4	63	OV 12VIN - RT9553B		
33	FAN TYPE-M SYSFAN5	64	ACPI - 3VSB / 5VDIMM		
34	LAN - RTL8111H	65	ATX Power - FrpntPanel / EMI		
35	LAN - RT8125B	66	LED - EZDEBUG / AMP		



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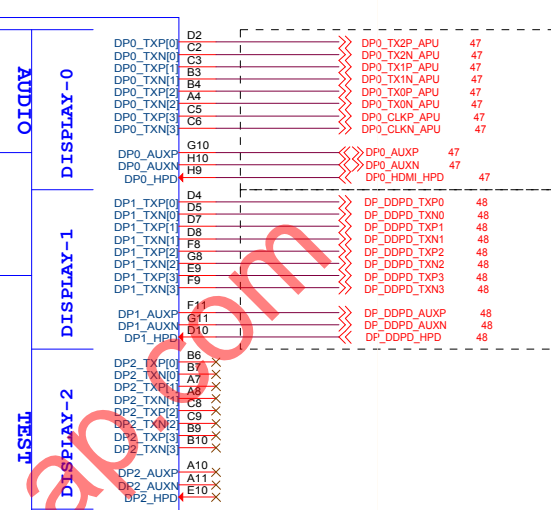
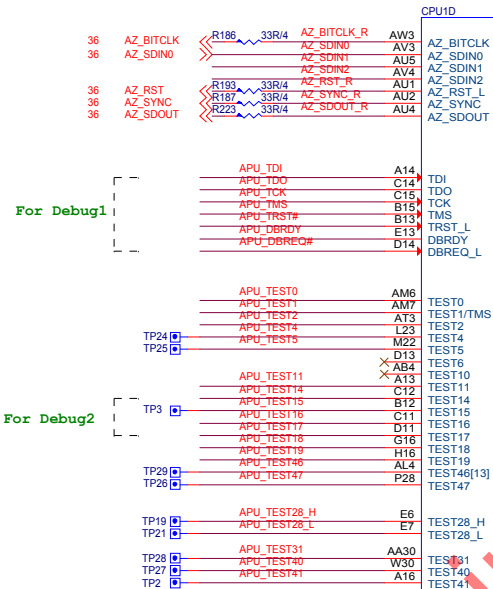
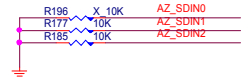
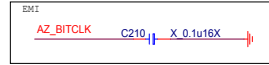
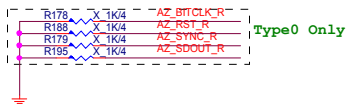
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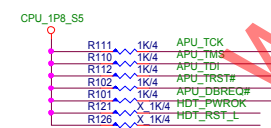
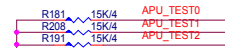
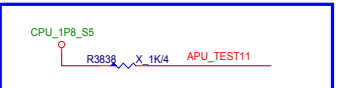
For HDMI

For DP

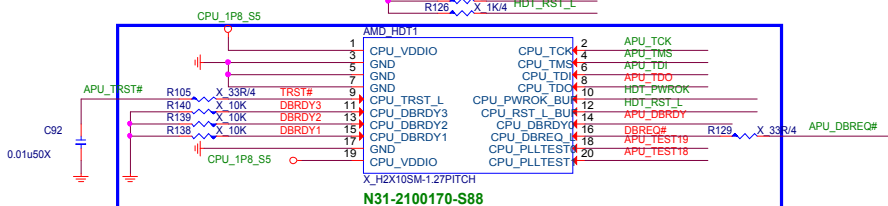
Not supported on TYPE 2/4

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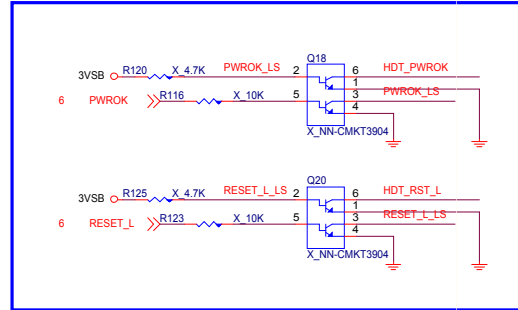
2020.04.06

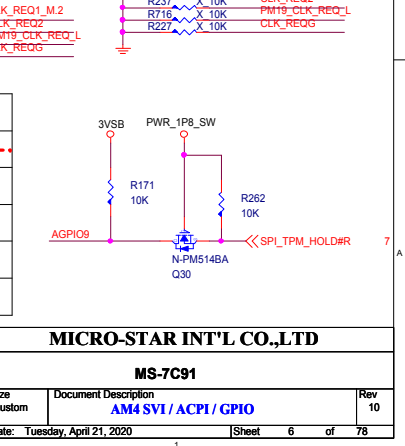
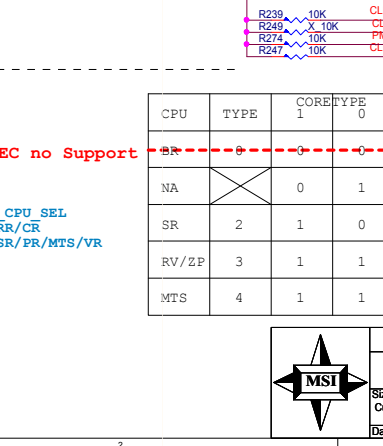
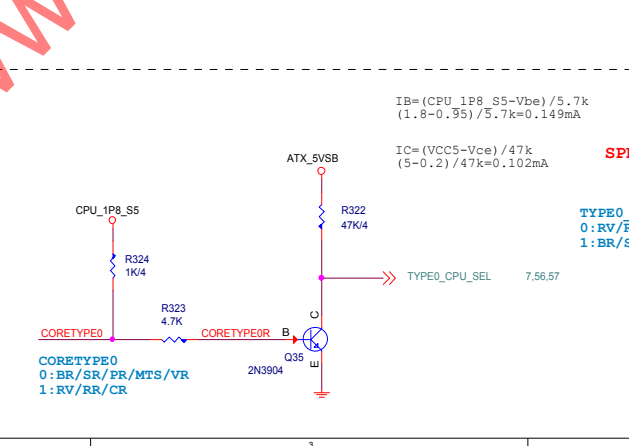
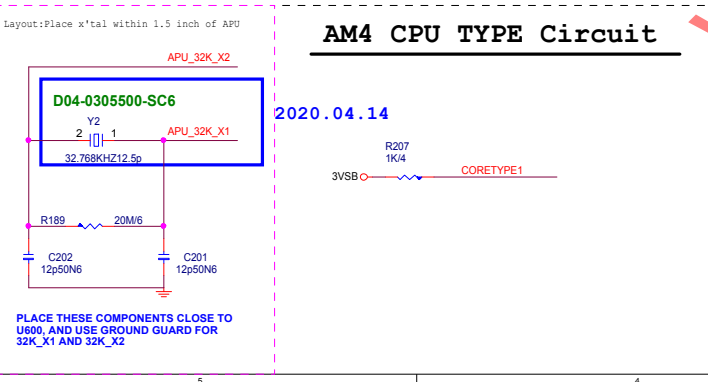
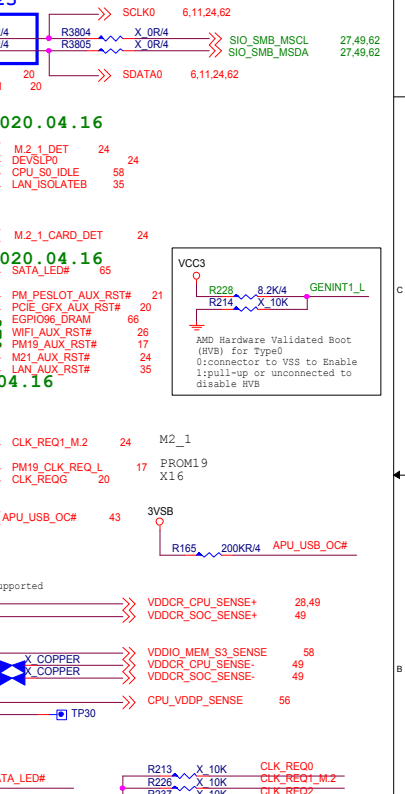
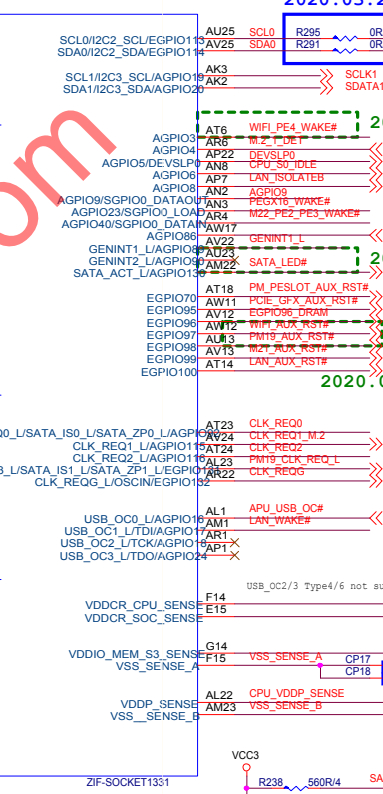
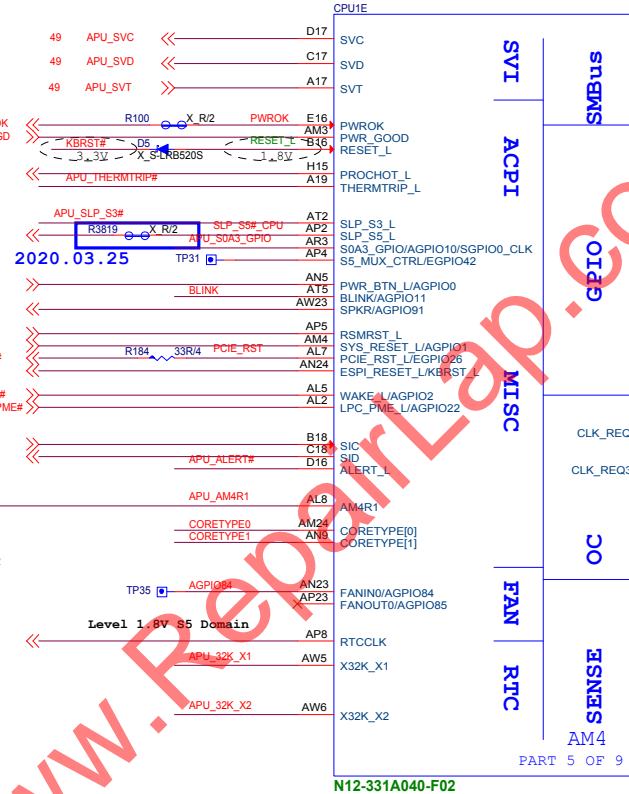
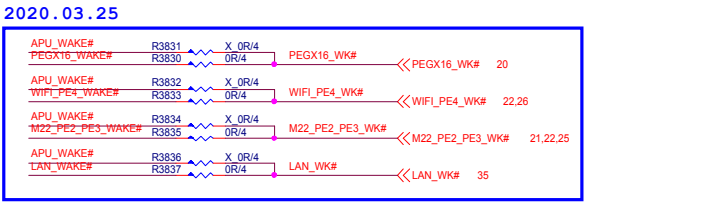
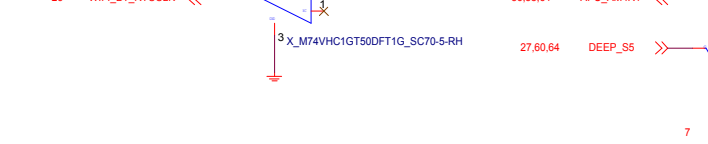
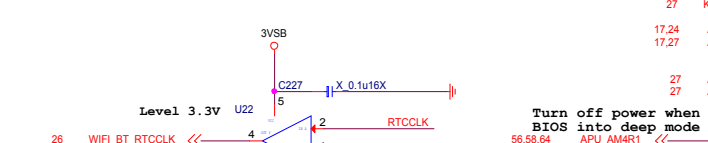
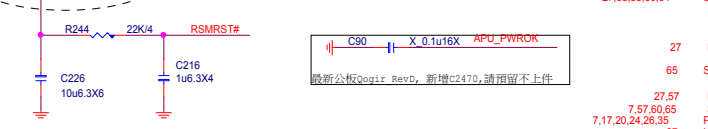
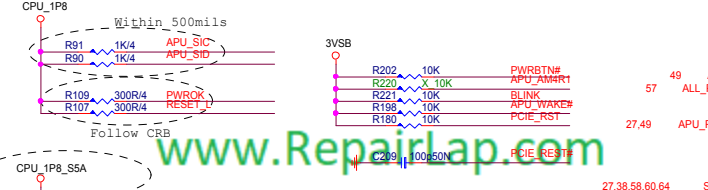
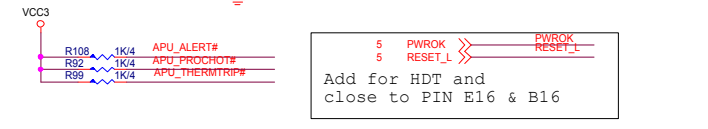
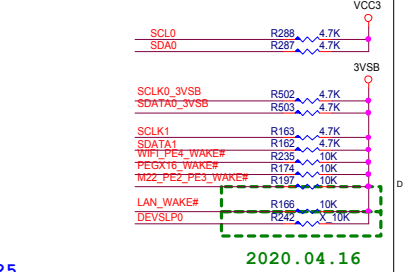
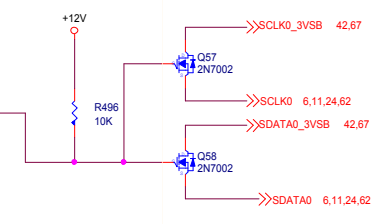
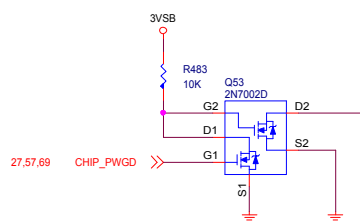
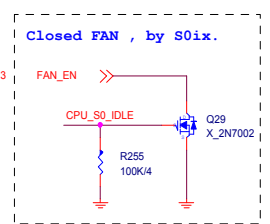
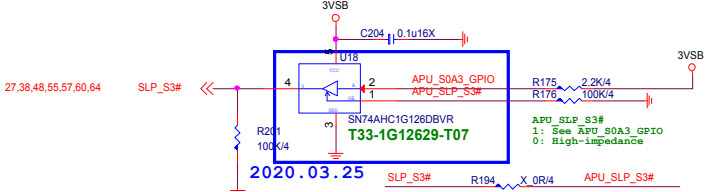


2020.04.06

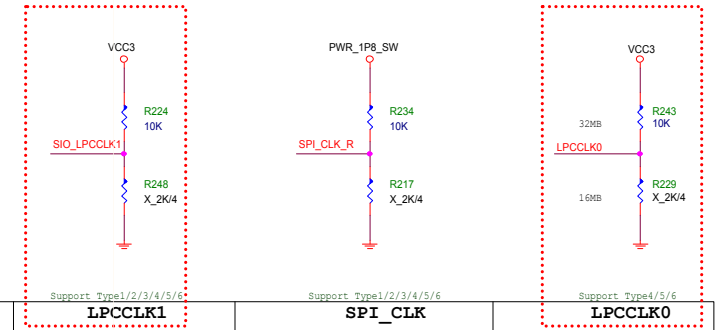


2020.04.06

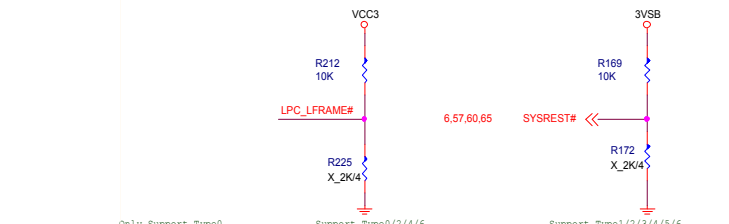




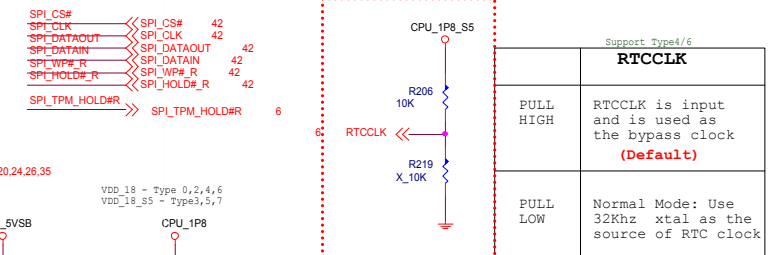
Strapping Options



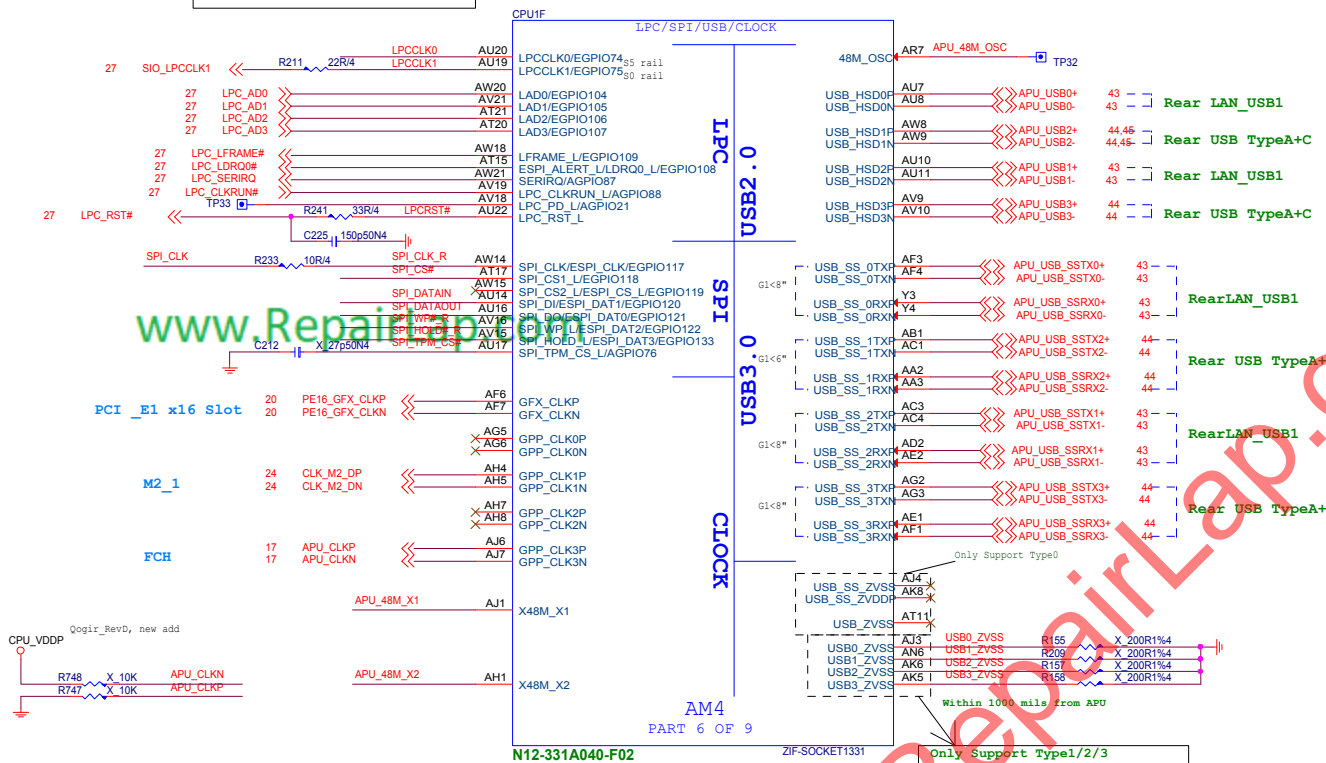
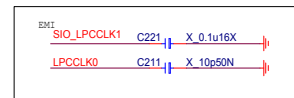
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image (Default)
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]



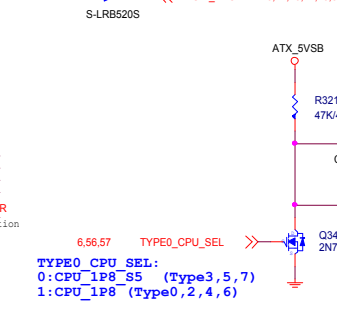
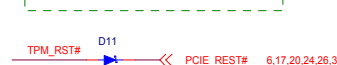
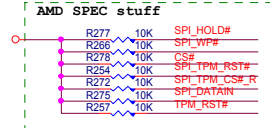
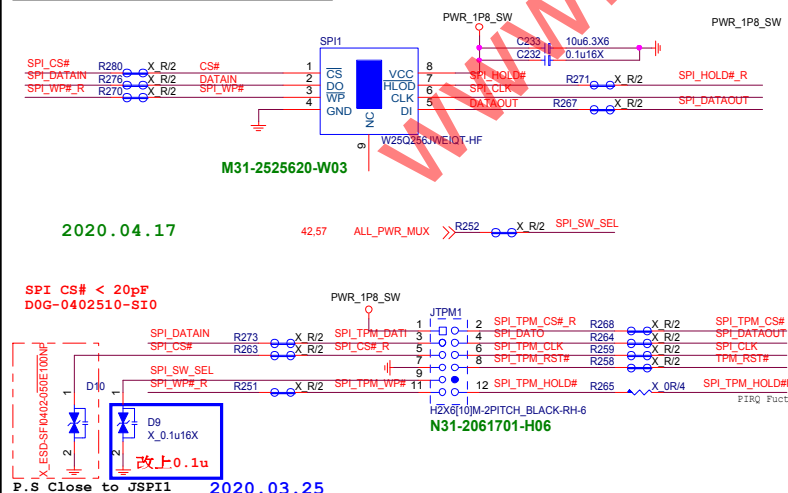
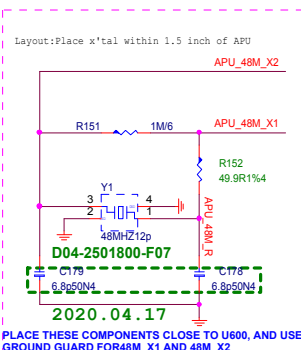
	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

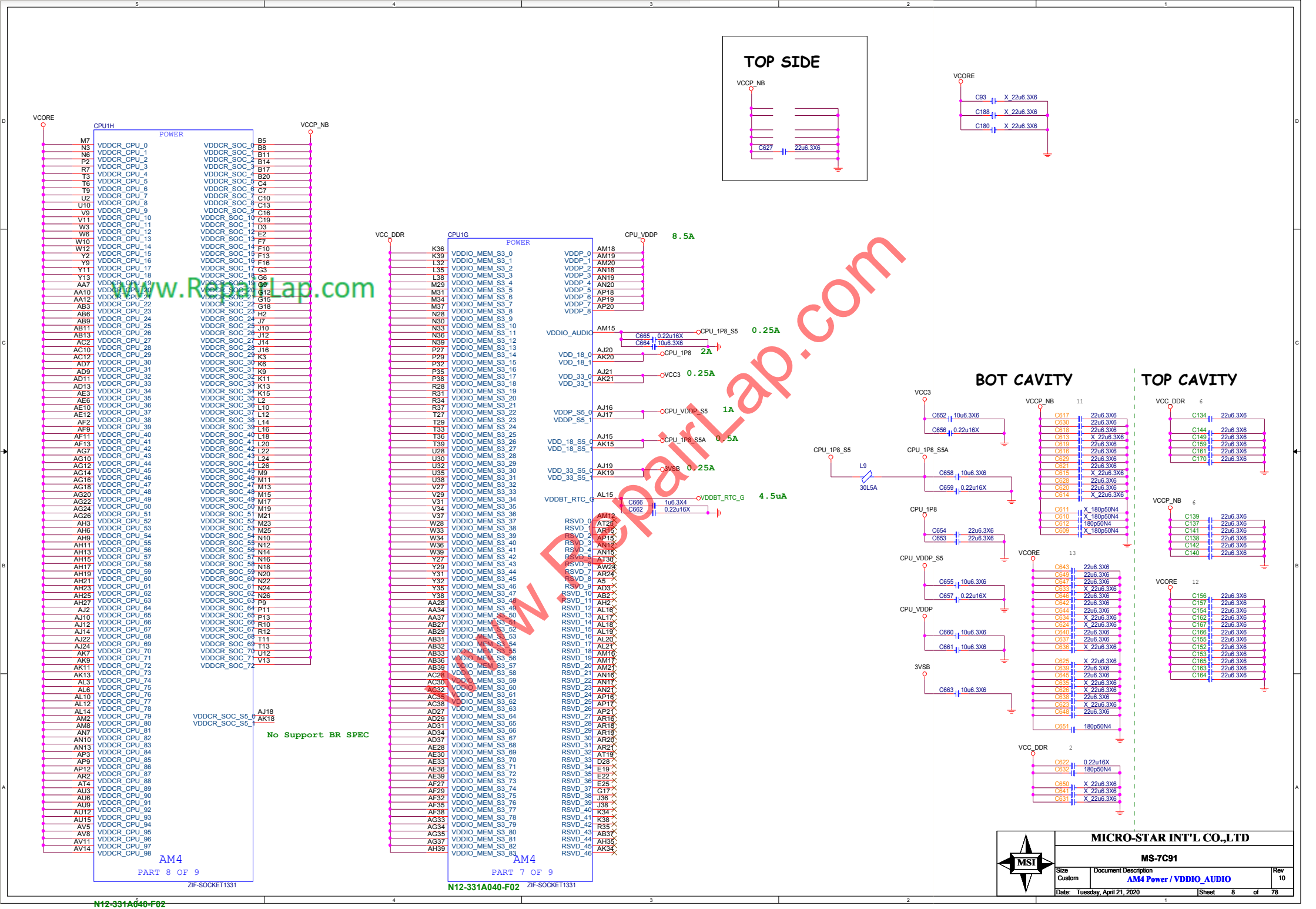


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SPI ROM (1.8V)





GND

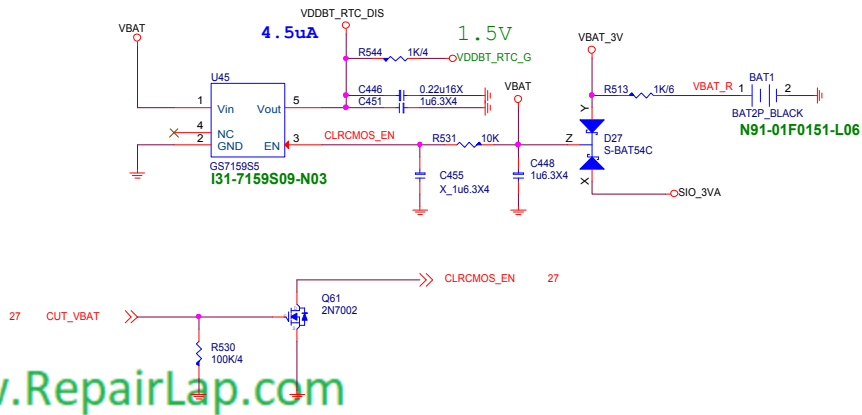


MICRO-STAR INT'L CO.,LTD

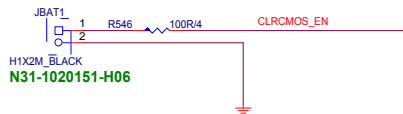
MS-7C91

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RTC & Clear CMOS Circuit

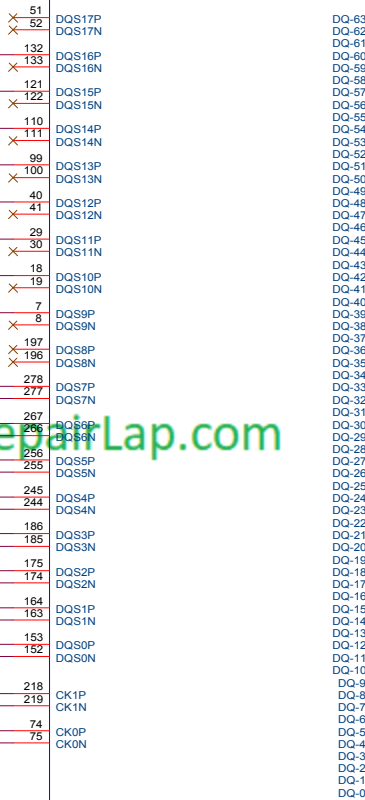
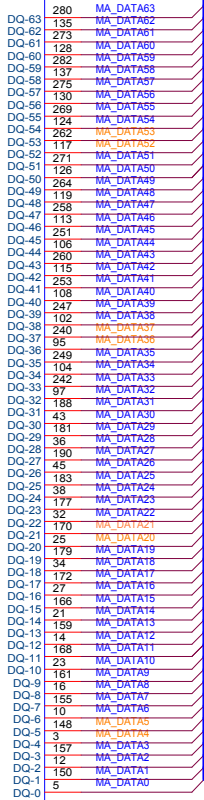


Clear CMOS button



A1 A2 B1 B2

DIMMA1A

235 C2
237 S3_N_C1
93 S2_N_C089 MA0_CS_L1
84 MA0_CS_L0
203 MA0_CKE1
60 MA0_CKE0
91 MA0_ODT1
87 MA0_ODT0199 CB-7
192 CB-6
191 CB-5
201 CB-4
56 CB-3
194 CB-2
49 CB-058 MA_RESET_L
78 MA_EVENT_L
208 MA_ALERT_L
62 MA_ACT_L
222 MA_PAROUT230 SAVE_N_NC
144 RFU-0
205 RFU-1
227 RFU-2DDRIV-288P_BLACK
N13-2881281-L06207 MA_BG1
63 MA_BG0
224 MA_BANK1
81 MA_BANK0234 MA_ADD_17
82 MA_ADD_16
86 MA_ADD_15
228 MA_ADD_14
232 MA_ADD_13
65 MA_ADD_12
210 MA_ADD_11
225 MA_ADD_10
66 MA_ADD_9
68 MA_ADD_8
211 MA_ADD_7
69 MA_ADD_6
213 MA_ADD_5
214 MA_ADD_4
71 MA_ADD_3
216 MA_ADD_2
72 MA_ADD_1
79 MA_ADD_0141 SMB_CLK_DIMM
285 SMB_DATA_DIMM238 SA-2
140 SA-1
139 SA-0DIMM1 (CHANNEL-A) -A0
ADDRESS = 0:0 [SA1:SA0]

<< MA_DATA[63..0] 3.11

56-63

48-55

40-47

32-39

24-31

16-23

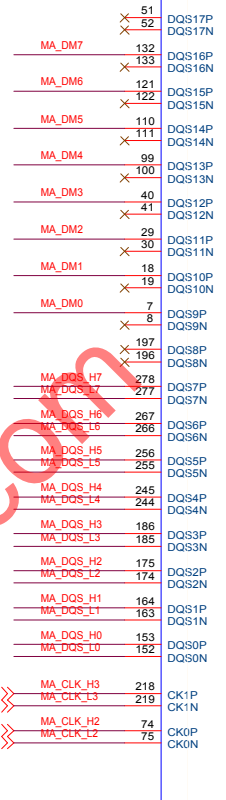
8-15

0-7

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2
DIMMB1	A6

6.24,62 SCLK0 SCLK0 R294 X R/2 SMB_CLK_DIMM
6.24,62 SDATA0 SDATA0 R290 X R/2 SMB_DATA_DIMM 12

DIMMA2A

235 C2
237 S3_N_C1
93 S2_N_C089 MA1_CS_L1
84 MA1_CS_L0
203 MA1_CKE1
60 MA1_CKE0
91 MA1_ODT1
87 MA1_ODT0199 CB-7
192 CB-6
191 CB-5
201 CB-4
56 CB-3
194 CB-2
49 CB-058 MA_RESET_L
78 MA_EVENT_L
208 MA_ALERT_L
62 MA_ACT_L
222 MA_PAROUT230 SAVE_N_NC
144 RFU-0
205 RFU-1
227 RFU-2DDRIV-288P_BLACK
N13-2881281-L06

<< MA_DATA[63..0] 3.11

56-63

48-55

40-47

32-39

24-31

16-23

8-15

0-7

207 MA_BG1
63 MA_BG0
224 MA_BANK1
81 MA_BANK0234 MA_ADD_17
82 MA_ADD_16
86 MA_ADD_15
228 MA_ADD_14
232 MA_ADD_13
65 MA_ADD_12
210 MA_ADD_11
225 MA_ADD_10
66 MA_ADD_9
68 MA_ADD_8
211 MA_ADD_7
69 MA_ADD_6
213 MA_ADD_5
214 MA_ADD_4
71 MA_ADD_3
216 MA_ADD_2
72 MA_ADD_1
79 MA_ADD_0141 SMB_CLK_DIMM
285 SMB_DATA_DIMM238 SA-2
140 SA-1
139 SA-0DIMM2 (CHANNEL-A) -A4
ADDRESS = 1:0 [SA1:SA0]

VCC3_SPD

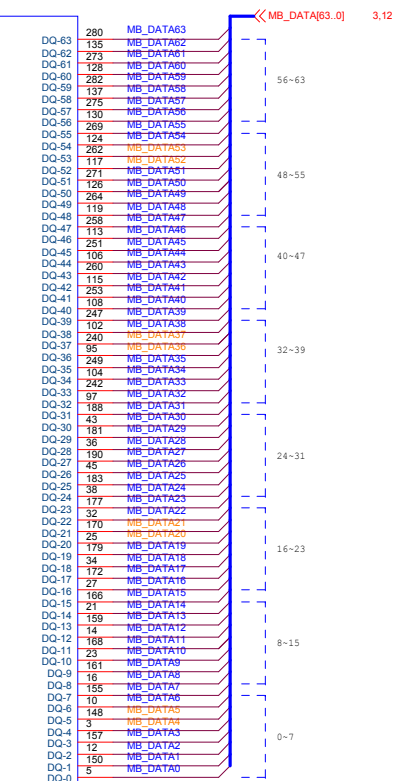
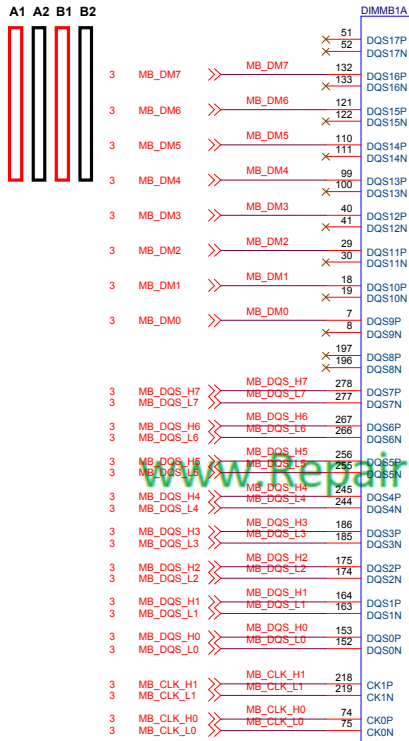
R283 1K/4



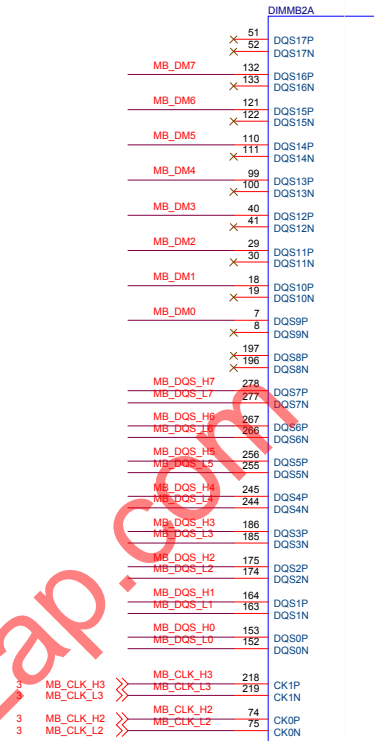
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DIMM3 (CHANNEL-B) -A2
ADDRESS = 0:1 [SA1:SA0]

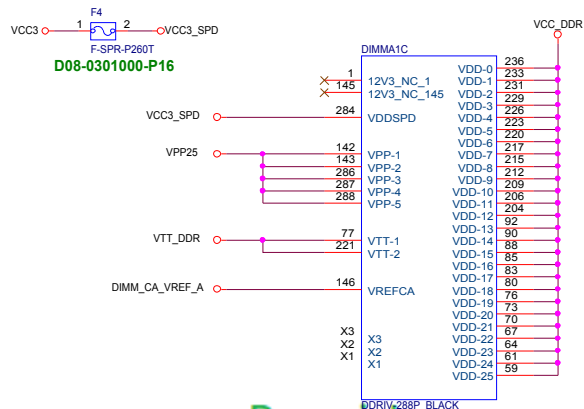


DIMM4 (CHANNEL-B) -A6
ADDRESS = 1:1 [SA1:SA0]

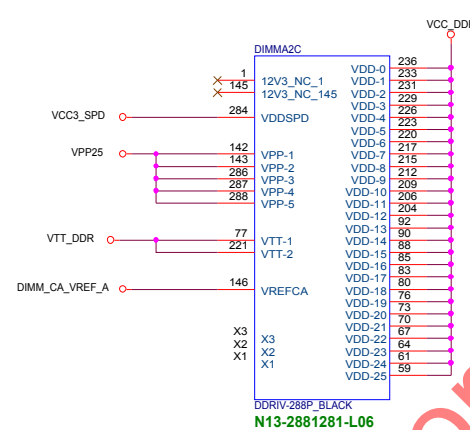


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Custom	DDR4 - DIMM CH-B	10	
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av1:D08-0301100-B07

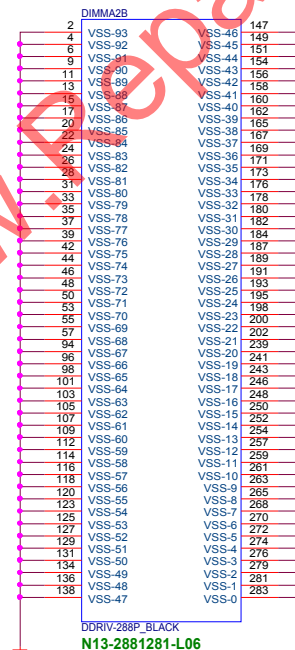
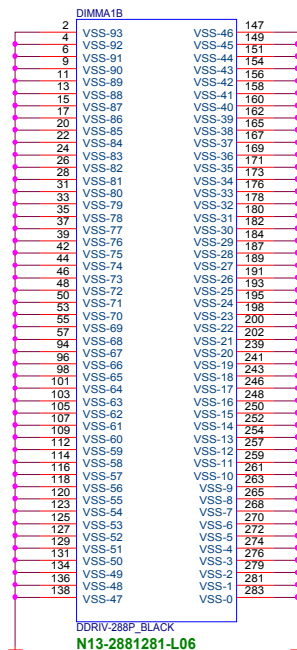
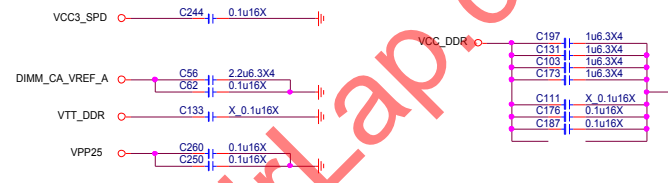
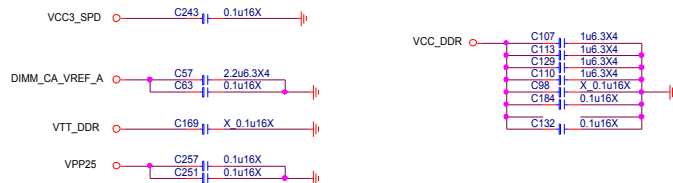
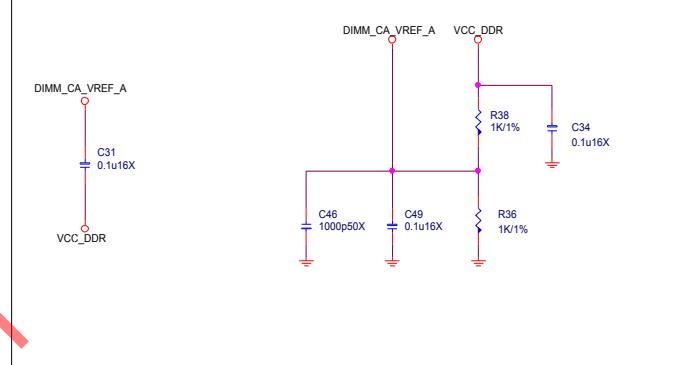


DIMM SLOT PN BY SPEC



DDR VREF

(place resistors close to DIMMs)



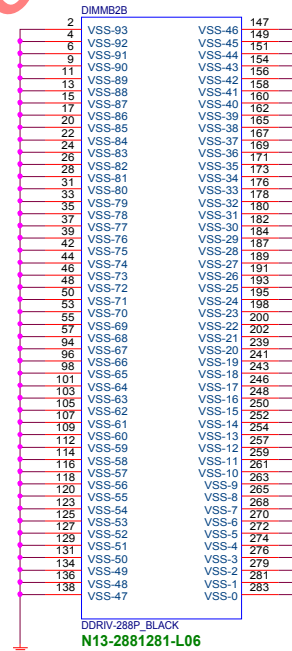
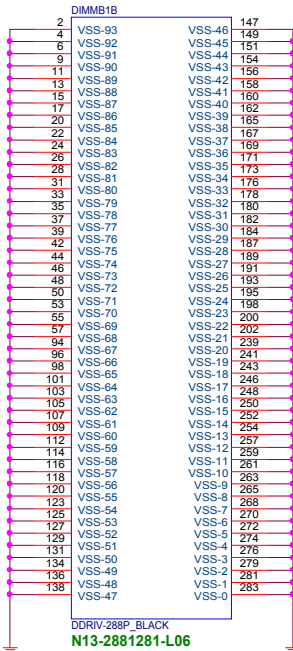
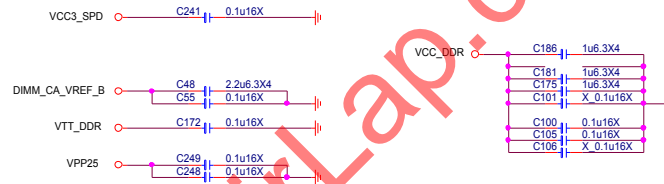
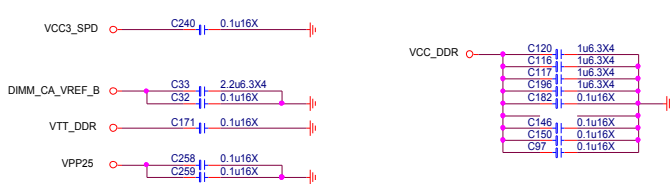
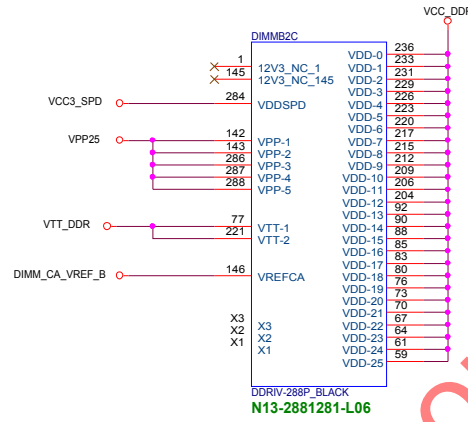
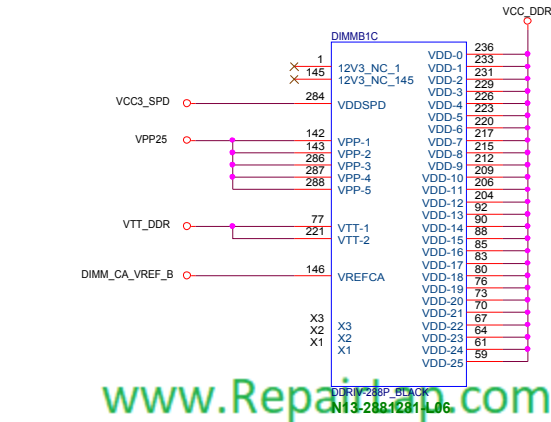
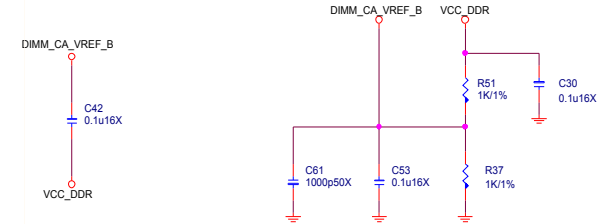
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DDR VREF

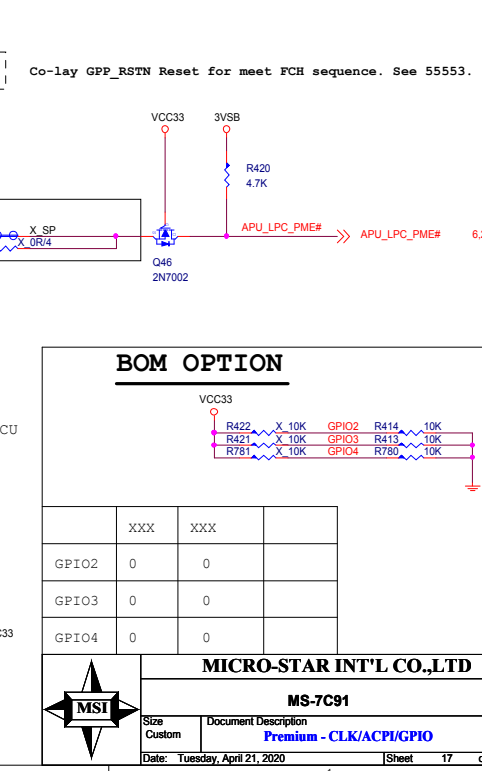
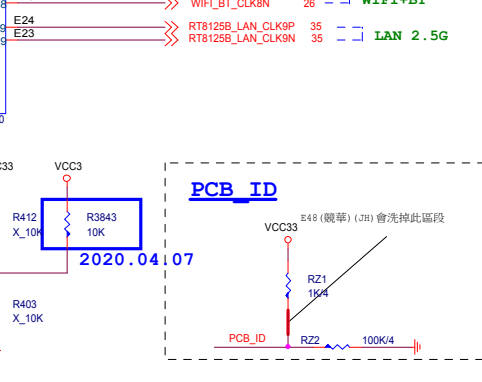
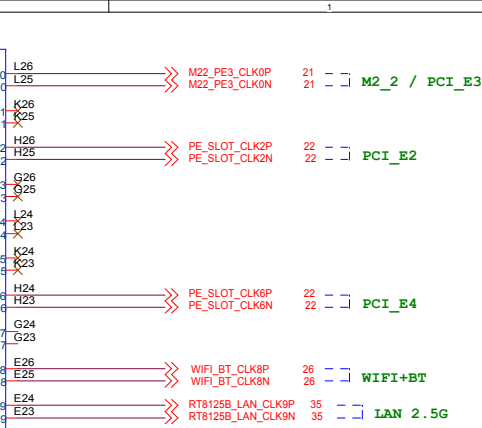
(place resistors close to DIMMs)

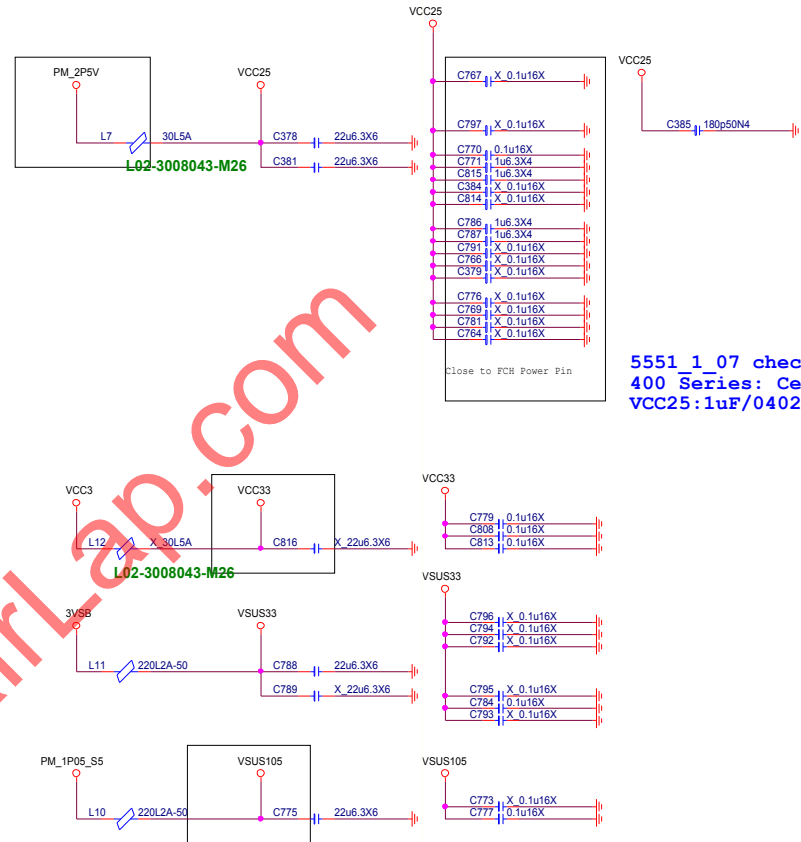
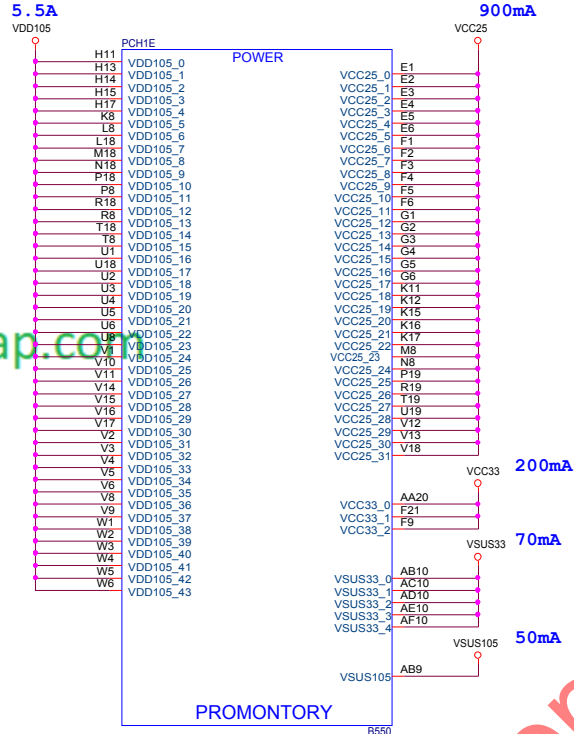
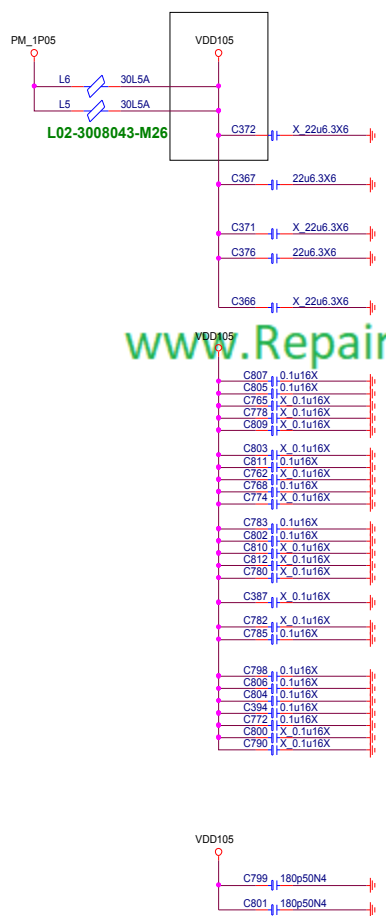


MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	DDR4 - POWER/GND-2	10
Date: Tuesday, April 21, 2020	Sheet 14 of 78	

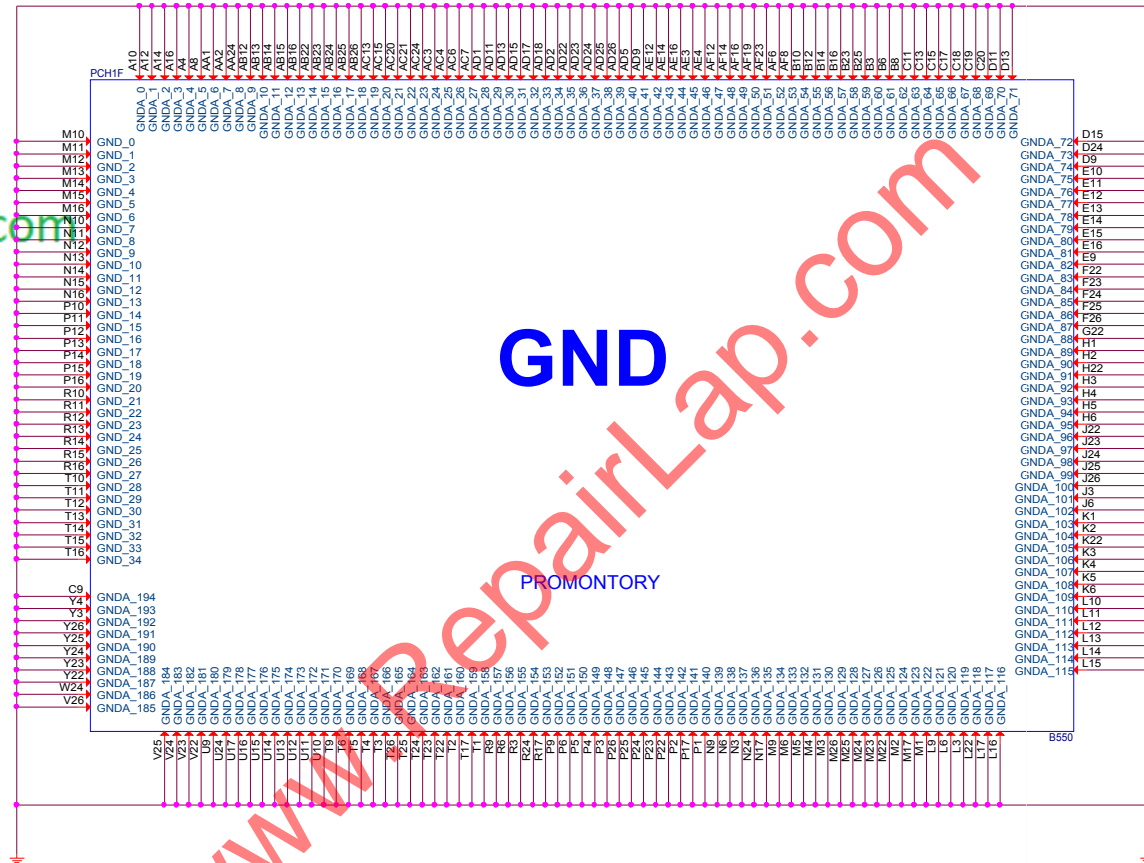




5551_1_07 check list
400 Series: Ceramic capacitors.
VCC25:1uF/0402

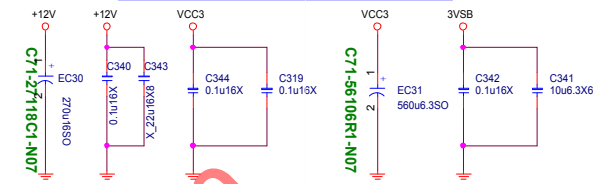
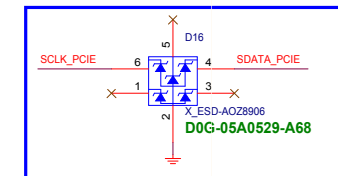
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www.RepairLap.com

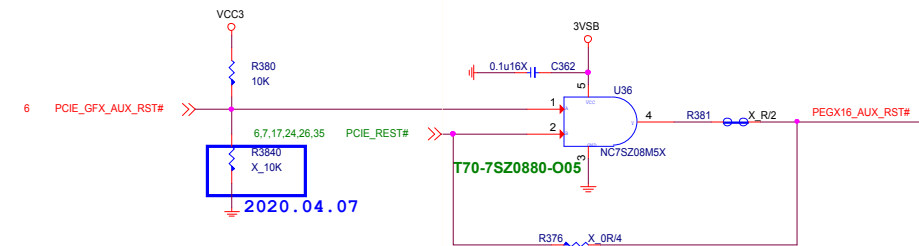
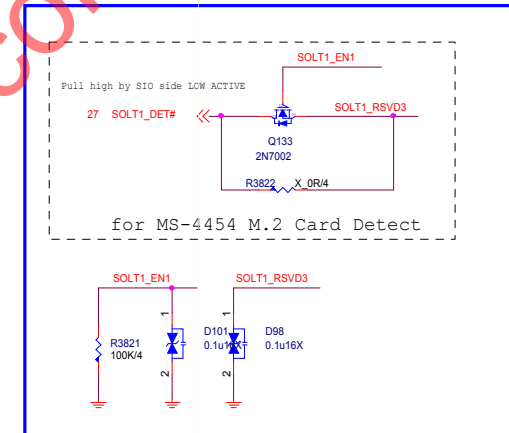


PCI_E1

SMB_SEL
GPIO Default High



2020.03.25



+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

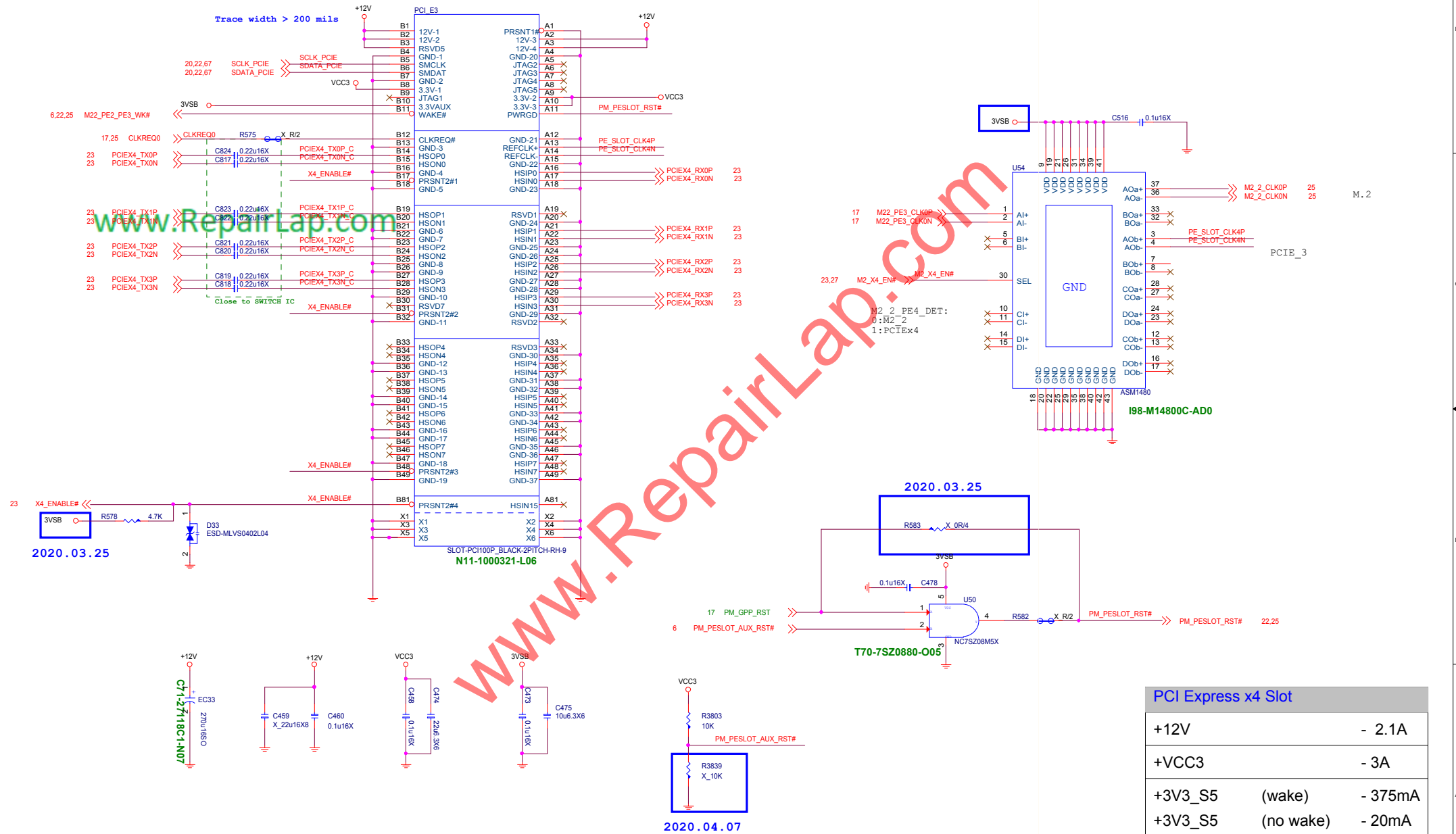


MS-7C91

Size Custom	Document Description PCI_E2 (X16)	Rev 10
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PCI EXPRESS x4 SLOT

PCI_E3 X4



PCI Express x4 Slot		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA



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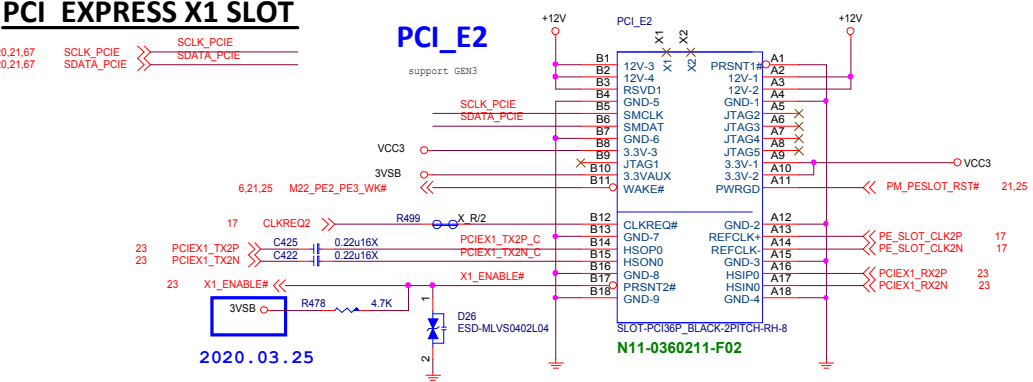
Size	Document Description	Rev
Custom	PCI_E3 (X4)	10
Date: Tuesday, April 21, 2020		Sheet 21 of 78

PCI EXPRESS X1 SLOT

20,21,67 SCLK_PCIE
20,21,67 SDATA_PCIE

PCI_E2

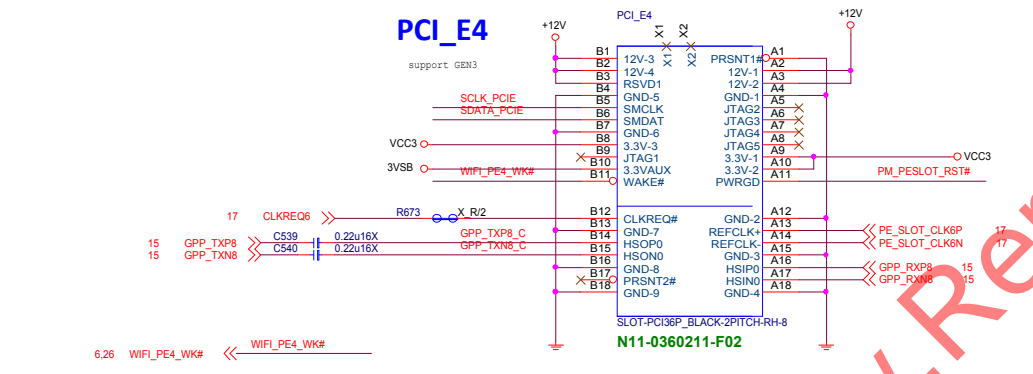
support GEN3




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PCI_E4

support GEN3



PCI Express x1 Slot *3	
+12V	- 1.5 A
+VCC3	- 9A
+3V3_S5 (wake)	- 1.125A
+3V3_S5 (no wake)	- 20mA



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MS-7C91

Size	Document Description	Rev
Custom	PCI_E2/E4_X1	10
Date:	Tuesday, April 21, 2020	Sheet 22 of 78

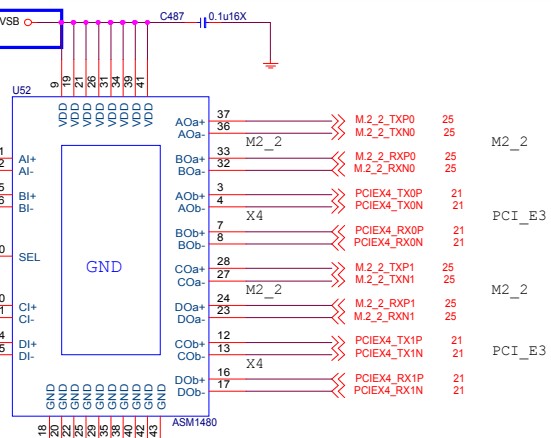
SEL	Function
L	N_in +/1 to N_out+/-
H	N_in +/1 to N_outb+/-

M2_2 PE4_DET:
0:M2_2
1:PCIeX4

M2_X4_EN# 30

GPP_TXP0 15
GPP_TXN0 15
GPP_RXP0 15
GPP_RXN0 15

GPP_TXP1 15
GPP_TXN1 15
GPP_RXP1 15
GPP_RXN1 15



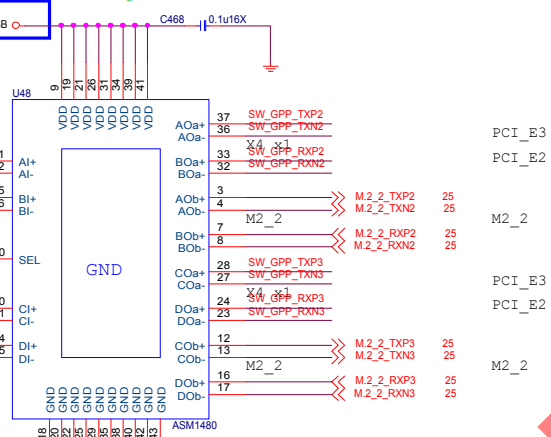
www.RepairLap.com

M2_2 X4X1_DET:
0:PCI_E3 & PCI_E2
1:M2_2

M2_X4_X1_EN# 30

GPP_TXP2 15
GPP_TXN2 15
GPP_RXP2 15
GPP_RXN2 15

GPP_TXP3 15
GPP_TXN3 15
GPP_RXP3 15
GPP_RXN3 15

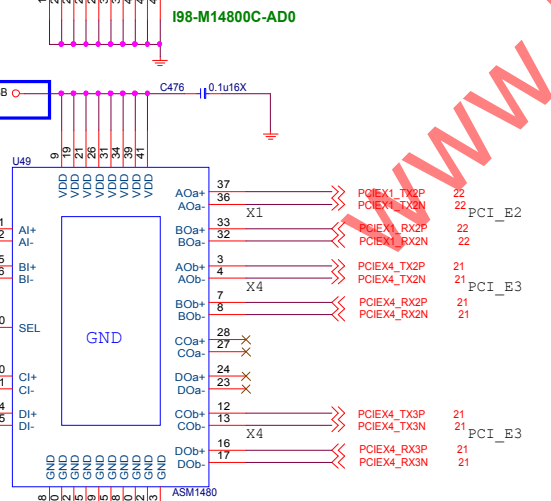


X4 X1 PE_DET:
0:PCI_E2 X1
1:PCI_E3 X4

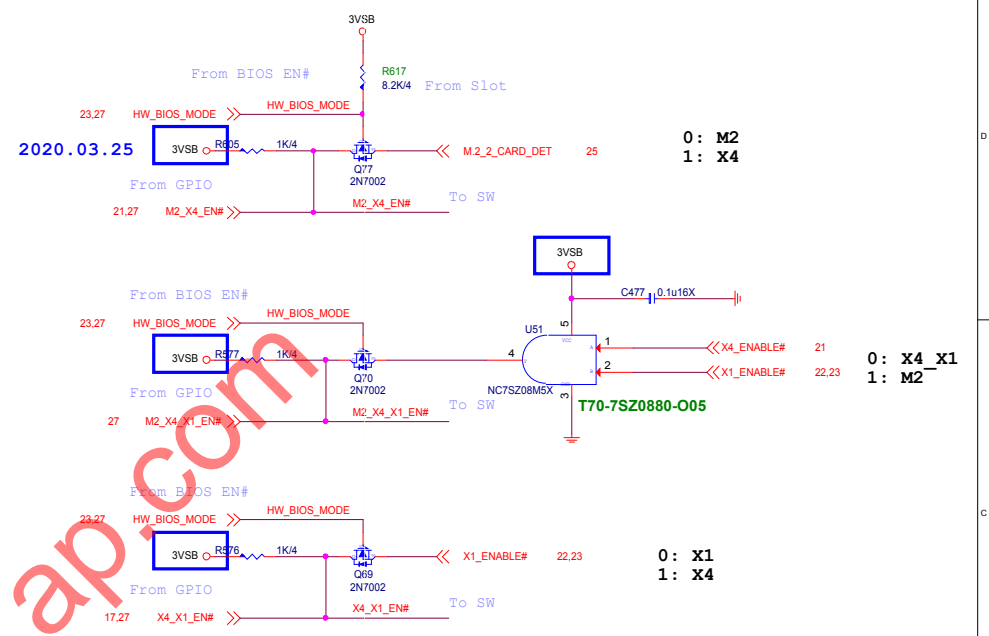
X4_X1_EN# 30

SW_GPP_TXP2 15
SW_GPP_TXN2 15
SW_GPP_RXP2 15
SW_GPP_RXN2 15

SW_GPP_TXP3 15
SW_GPP_TXN3 15
SW_GPP_RXP3 15
SW_GPP_RXN3 15



PCIe Lanes control circuit



HW_BIOS_MODE = High (HW MODE)

DEVICE	M2_2 X4	●(4)	X	X	●(2)	●(2)	X	X	●(2)
	PCI_E3 X4	X	●(4)	X	●(0)	X	●(2)	X	●(0)
	PCI_E2 X1	X	X	●(1)	X	●(1)	●(1)	X	●(1)
DETECT	M.2_2_CARD_DET	0	1	1	0	0	1	1	0
	X1_ENABLE#	1	1	0	1	0	0	1	0
	X4_ENABLE#	1	0	1	0	1	0	1	0

●(X) = availability Lanes number

HW_BIOS_MODE = Low (BIOS MODE)

BIOS GPIO SWITCH	M2_X4_EN#	0	0	0	0	1	1	1	1
	M2_X4_X1_EN#	0	0	1	1	0	0	1	1
	X4_X1_EN#	0	1	0	1	0	1	0	1
DEVICE	M2_2 X4	●(2)	●(2)	●(4)	●(4)	●(0)	●(0)	●(0)	●(0)
	PCI_E3 X4	●(0)	●(0)	●(0)	●(0)	●(2)	●(4)	●(2)	●(2)
	PCI_E2 X1	●(1)	●(0)	●(0)	●(0)	●(1)	●(0)	●(0)	●(0)



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Size	Document Description	Rev	
Custom	PCIE GEN3 SWITCH	10	
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M.2 1 Connector

M2下方零件擺放限高要小於0.9mm的零件

VCC3 4.25A
Max: 14W

LANE REVERSE TO SUPPORT SATA SSD

2020.03.25

2020.03.25

2020.03.25

2020.03.25

2020.04.16

2020.03.25 SMBUS Level Shift IC

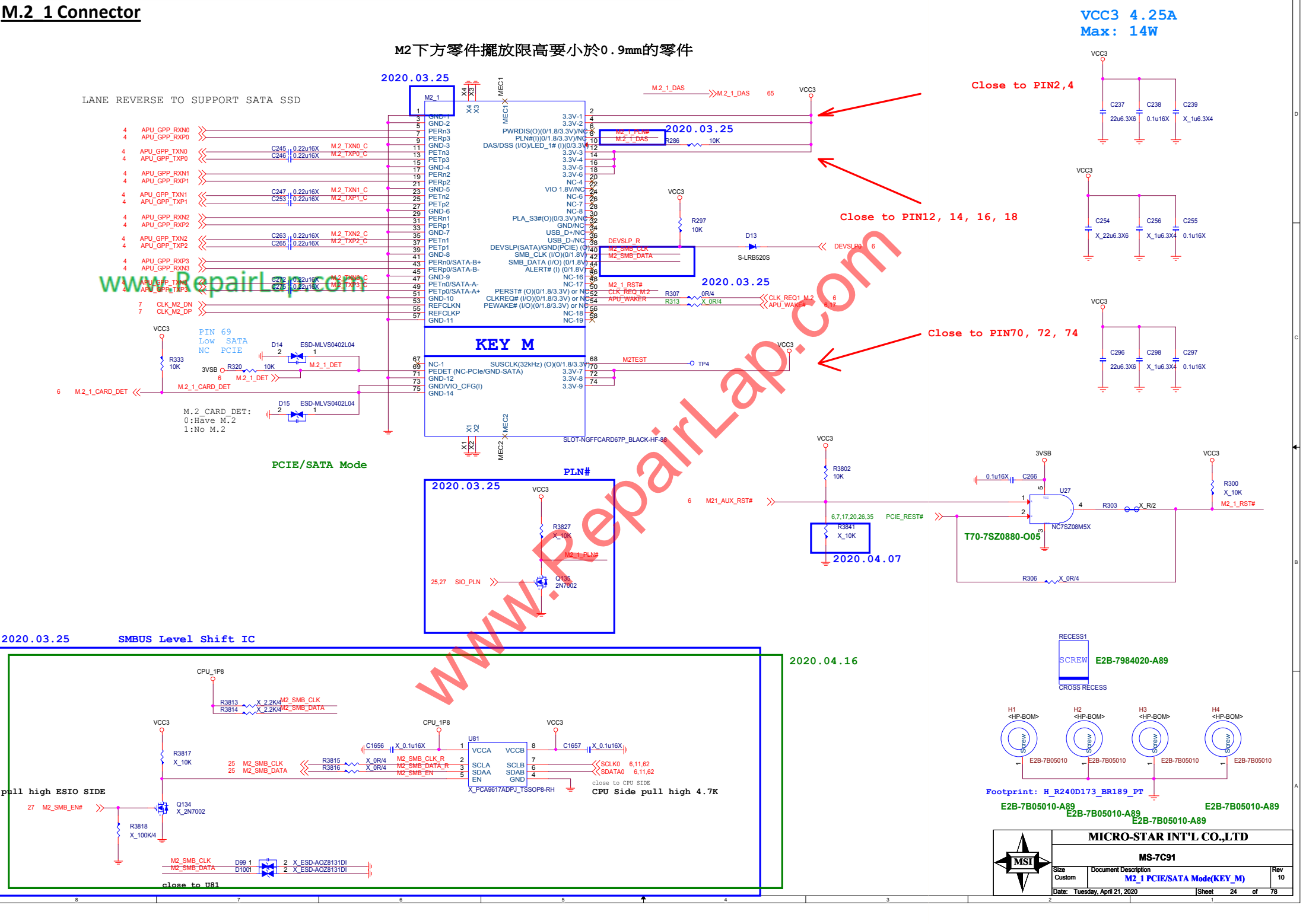
pull high ESIO SIDE

CPU Side pull high 4.7K

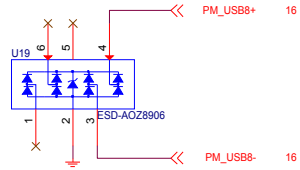
MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	M2_1 PCIE/SATA Mode(KEY_M)	10
Date: Tuesday, April 21, 2020	Sheet 24 of 78	

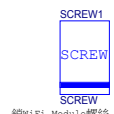
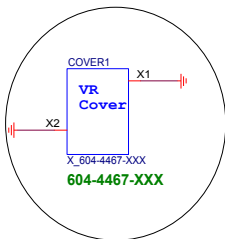
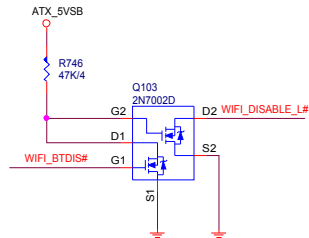
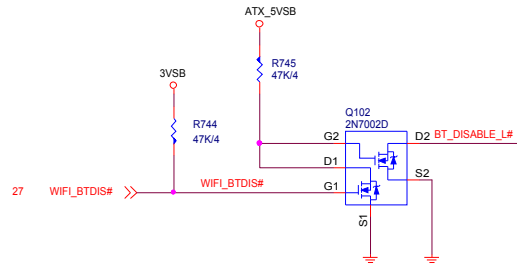


EMI NEAR CONNECTOR



3VSB C667 X 0.1u16X

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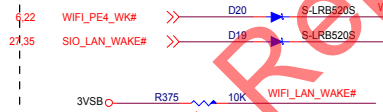
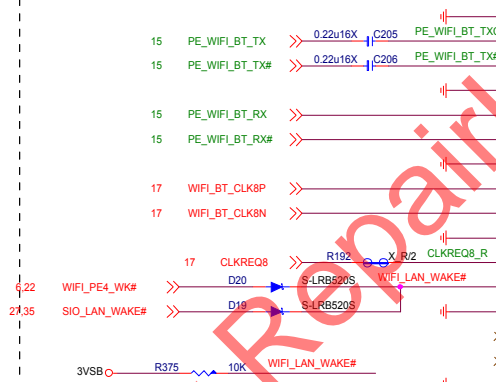
E43-1204046-P65



E43-1204046-P65

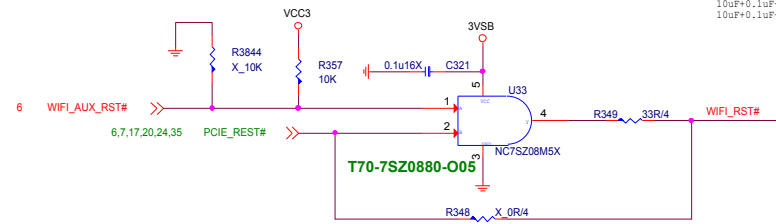


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KEY E

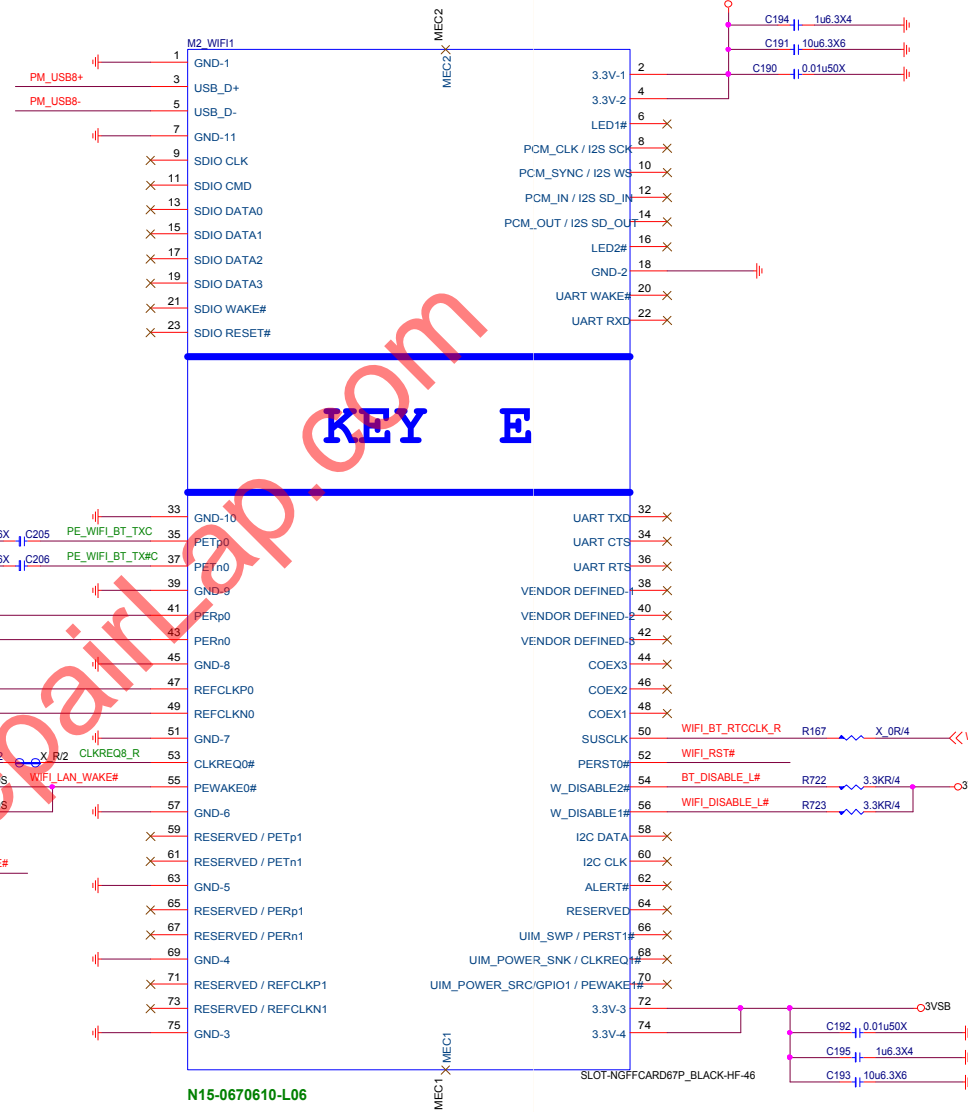
N15-0670610-L06



10uP+0.1uP+0.01uP at one end of socket in support of 3.3 V3V pins 2 and 4.
10uP+0.1uP+0.01uP at the other end of the socket in support of 3.3 V3V pins 70 and 72.

780mA

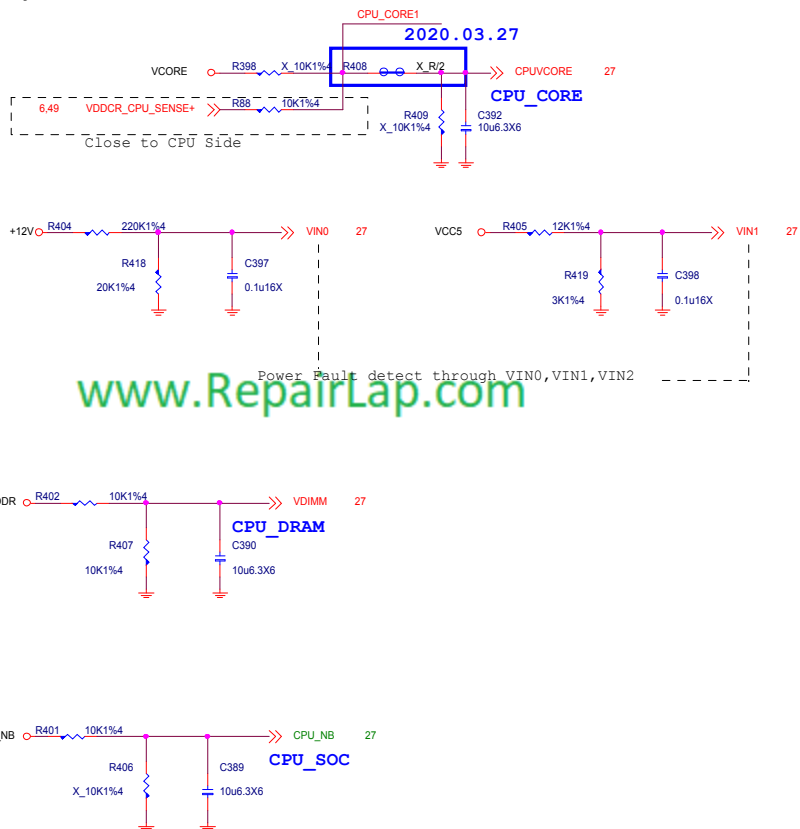
3VSB



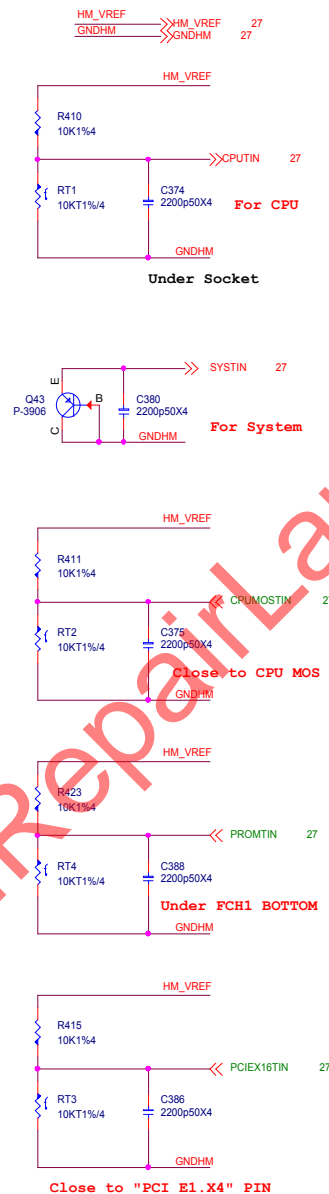
MICRO-STAR INT'L CO.,LTD			
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Custom	M2_2 - WIFI+BT	10	
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HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect



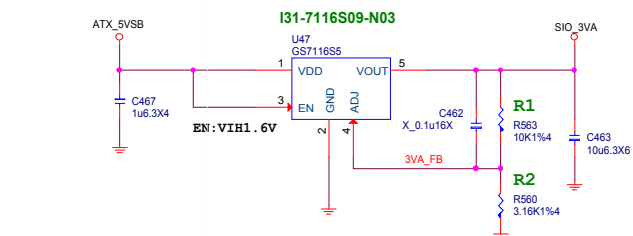
TEMP SENSOR



PM RESET

CPU RESET

SIO_3VA



$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (10K/3.16K)) \\ &= 3.33V \end{aligned}$$



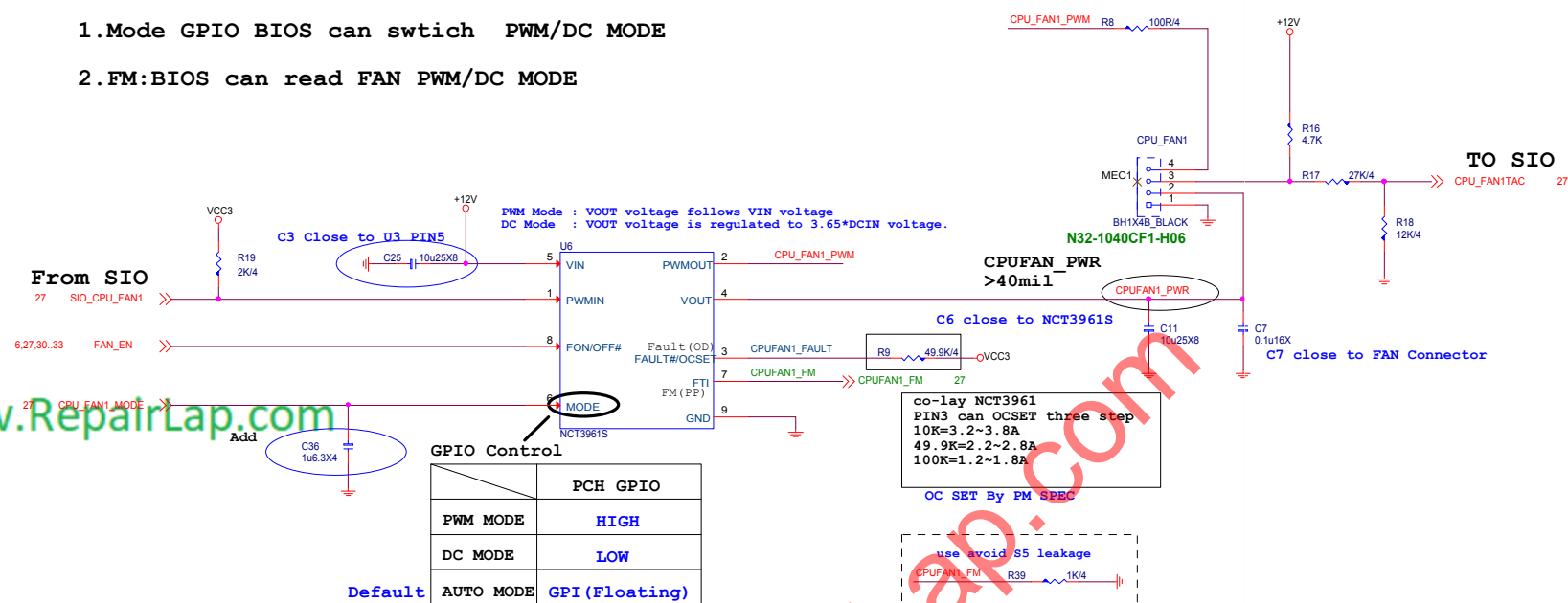
MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	SIO - HW Monitor	10
Date:	Tuesday, April 21, 2020	Sheet 28 of 78

```
TYPE N : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE
```

- 27 CPU_FAN1_MODE >>



MS-7C91

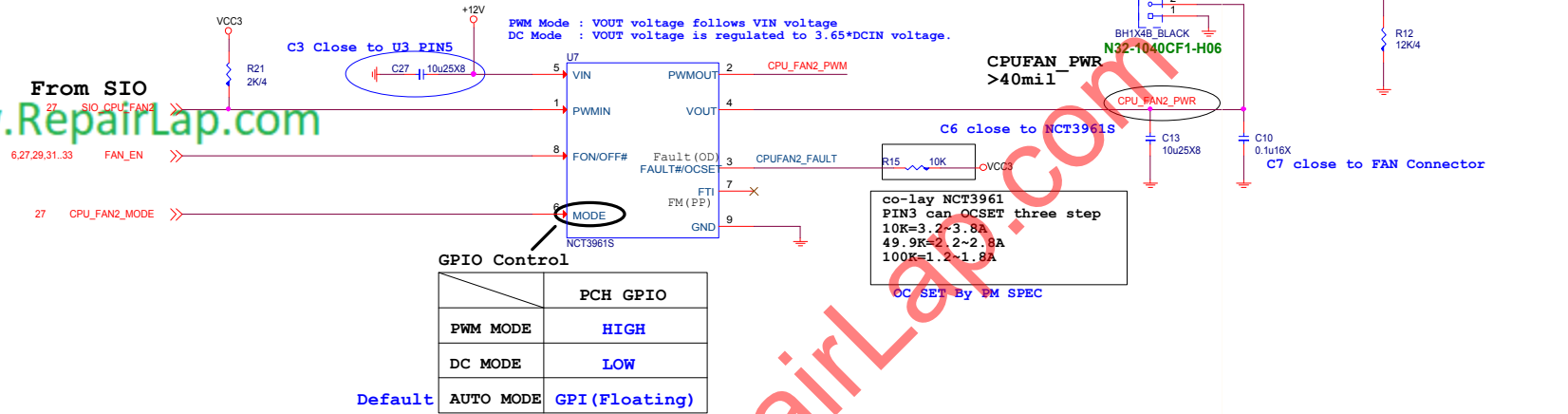
Size Custom	Document Description FAN TYPE-L CPUFANI	Rev 10
Date: Tuesday, April 21, 2020		Sheet 29 of 78

PUMPFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

From SIO
27 SIO_CPU_FAN2
www.RepairLap.com



MICRO-STAR INT'L CO.,LTD

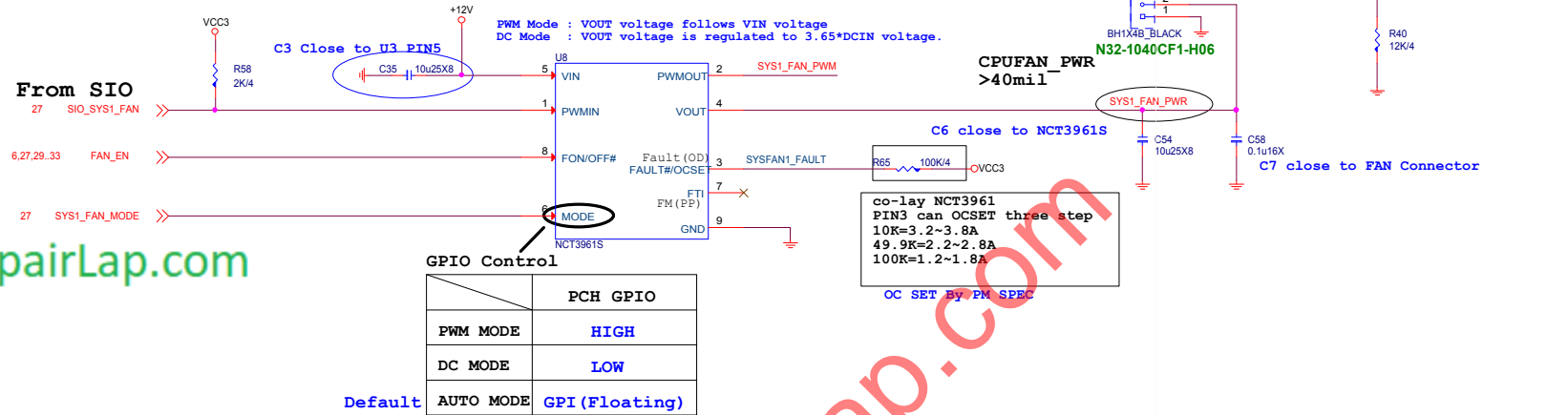
MS-7C91

Size	Document Description	Rev
Custom	FAN TYPE-K PUMPFANI	10
Date:	Tuesday, April 21, 2020	Sheet 30 of 78

SYSFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE

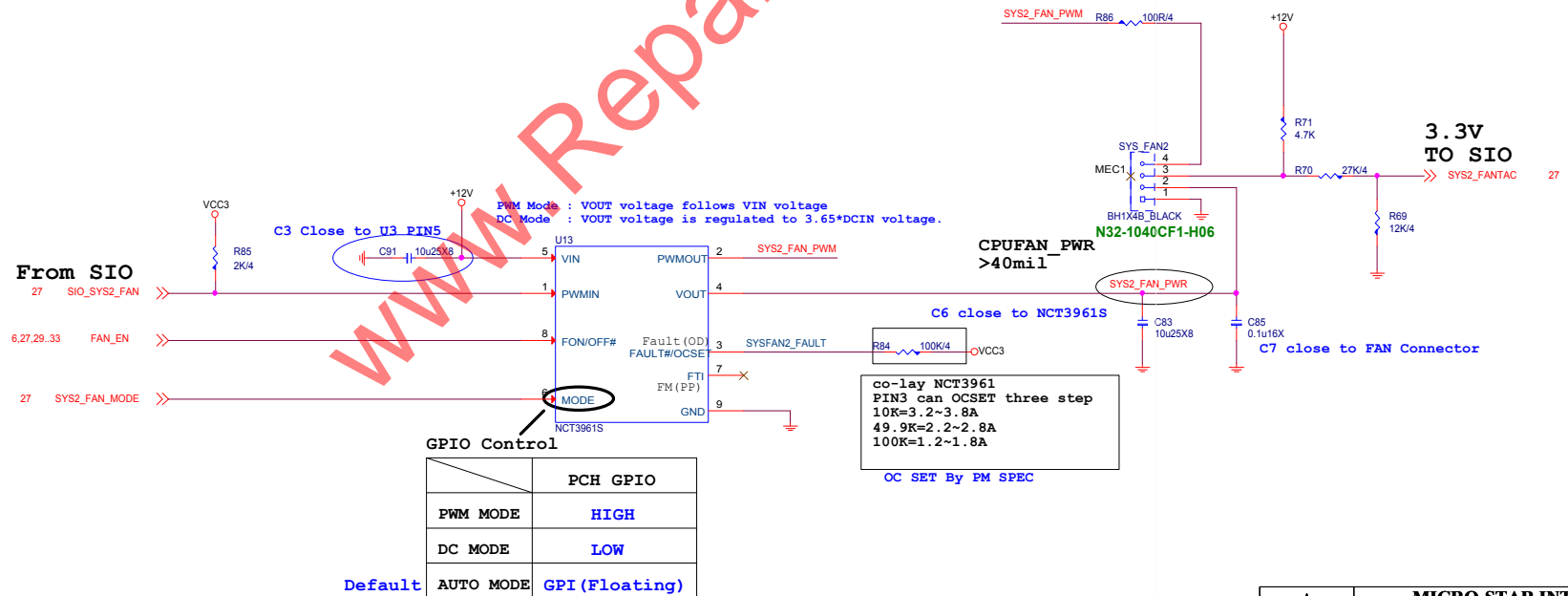


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SYSFAN2

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

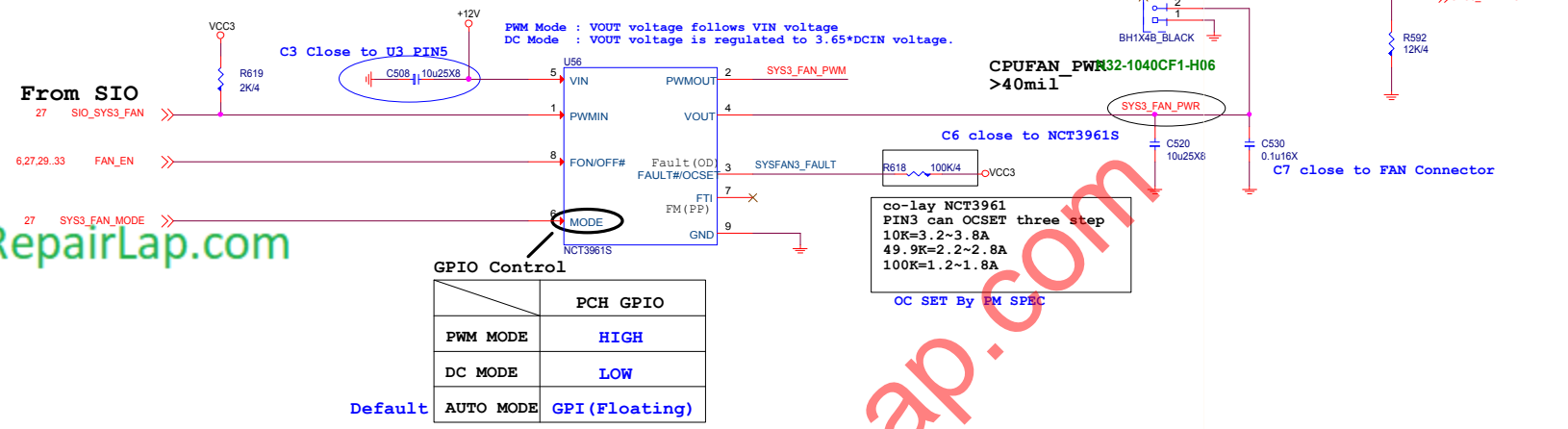
1.Mode GPIO BIOS can switch PWM/DC MODE



SYSFAN3

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

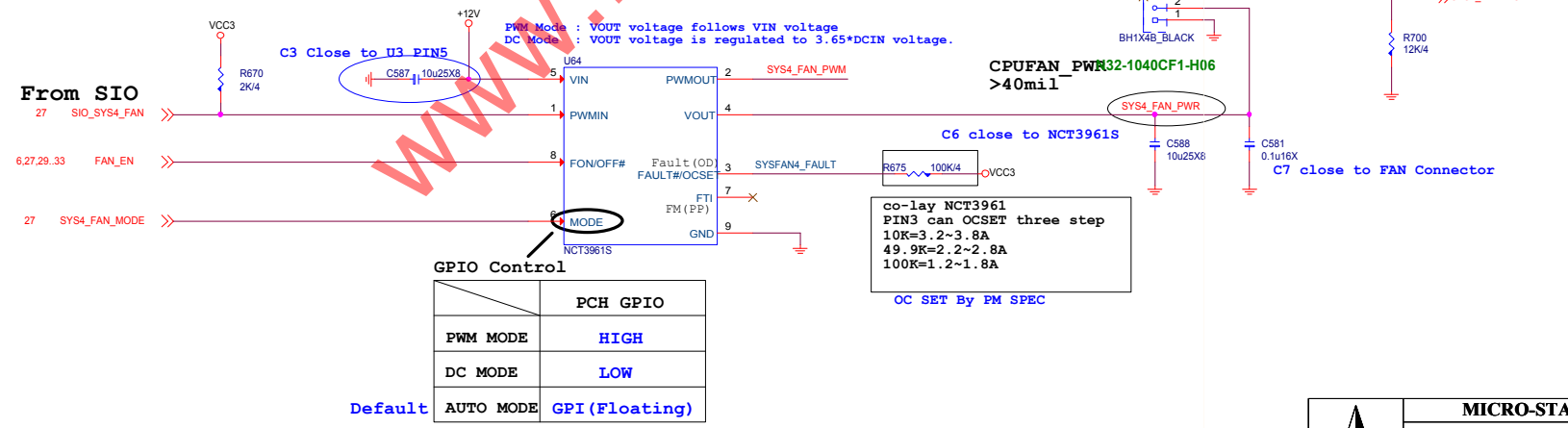
1.Mode GPIO BIOS can switch PWM/DC MODE



SYSFAN4

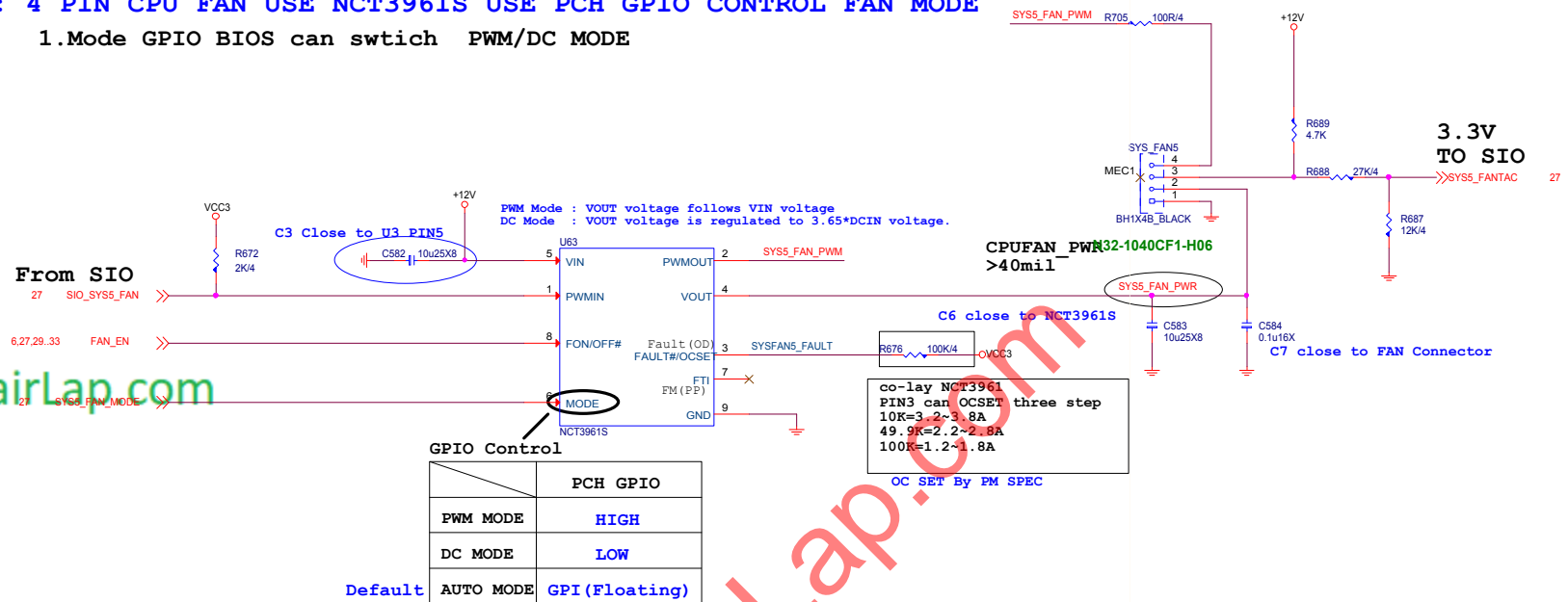
TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE



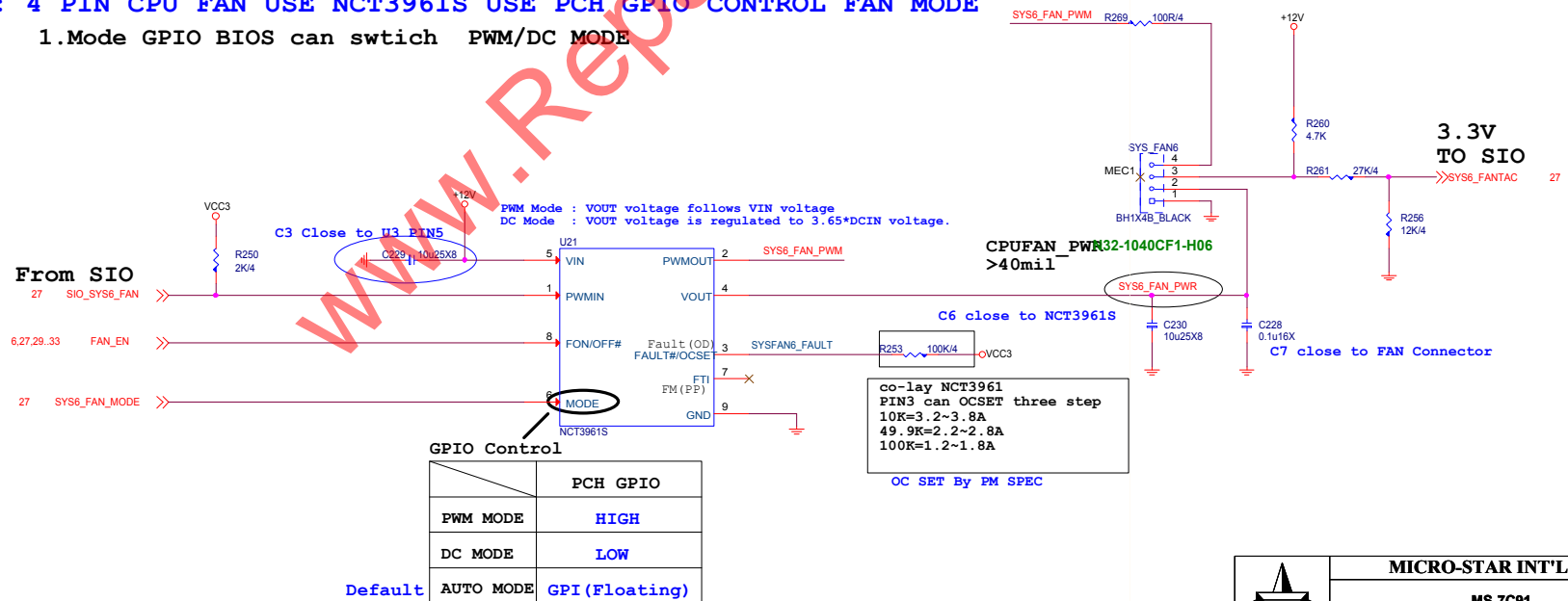
SYSFAN5 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE



SYSFAN6 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE

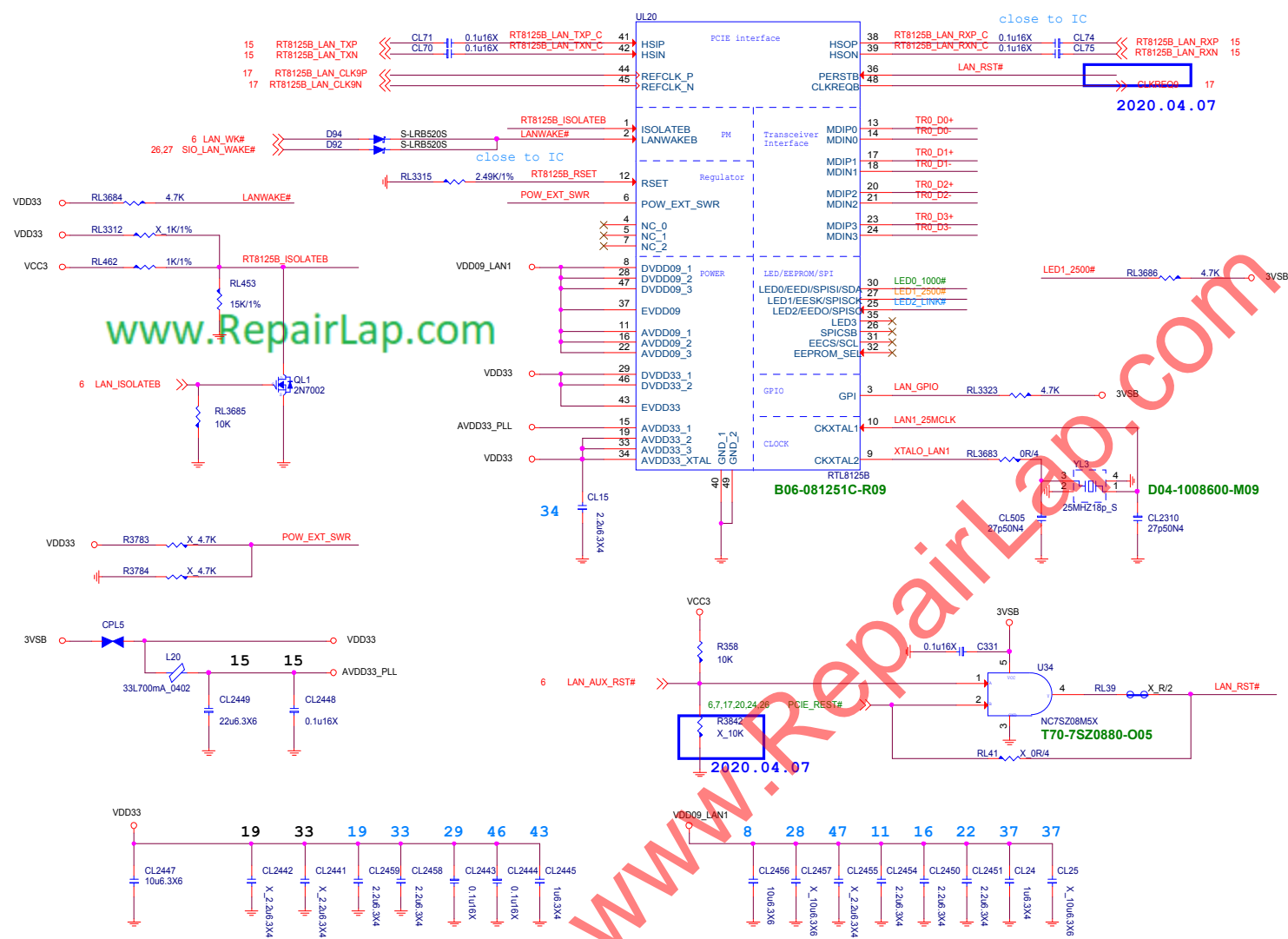


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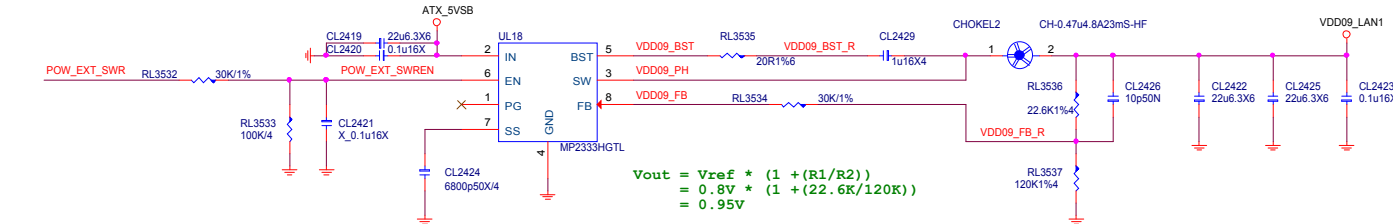
2020.04.16

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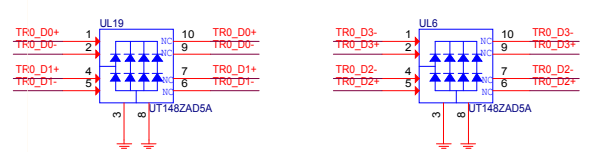
Realtek Lan1-RTL8125B(2.5G)



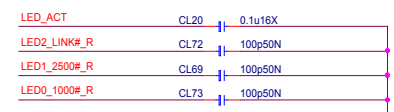
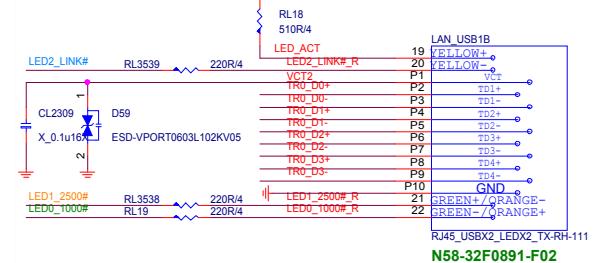
Input Current=(0.5*0.95)/5/0.8=0.12A



ESD Protect
close to connector



LAN Connector

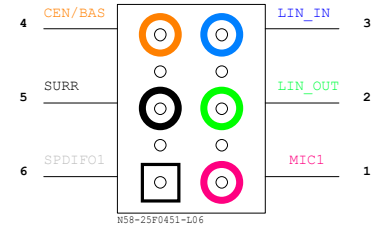
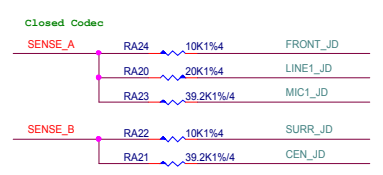
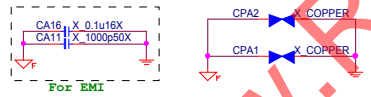
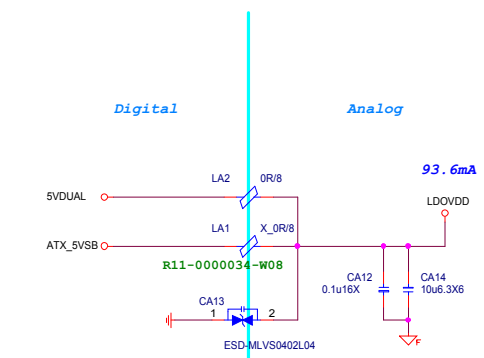
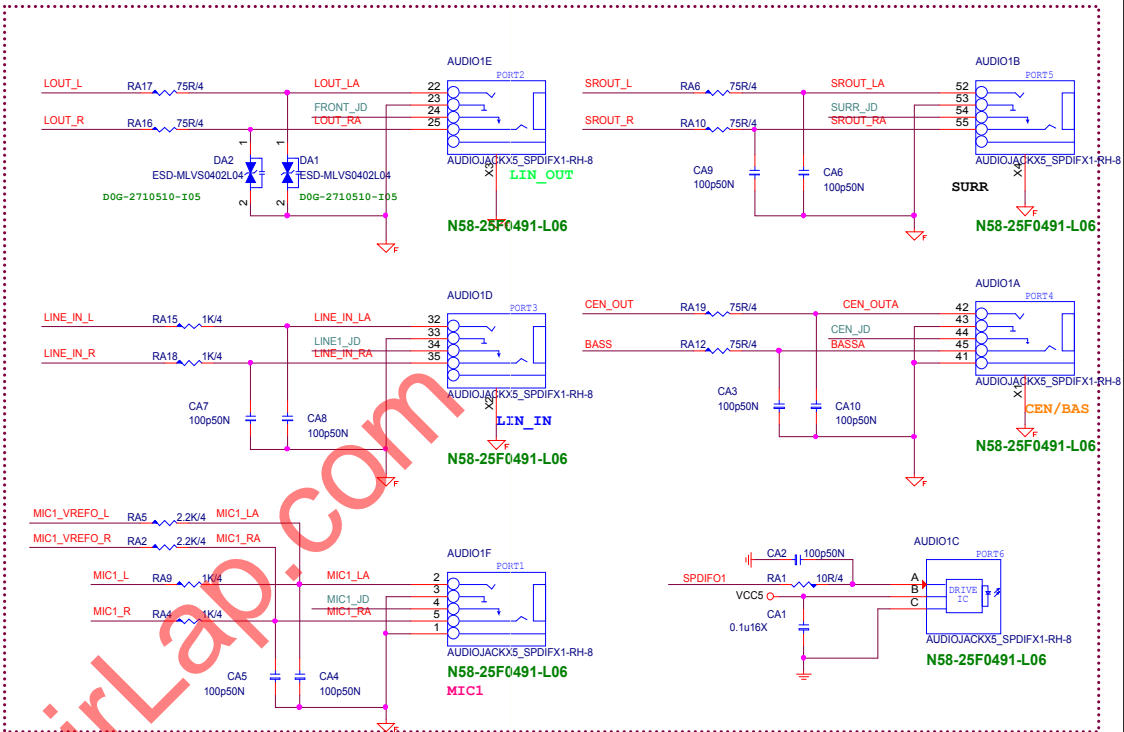
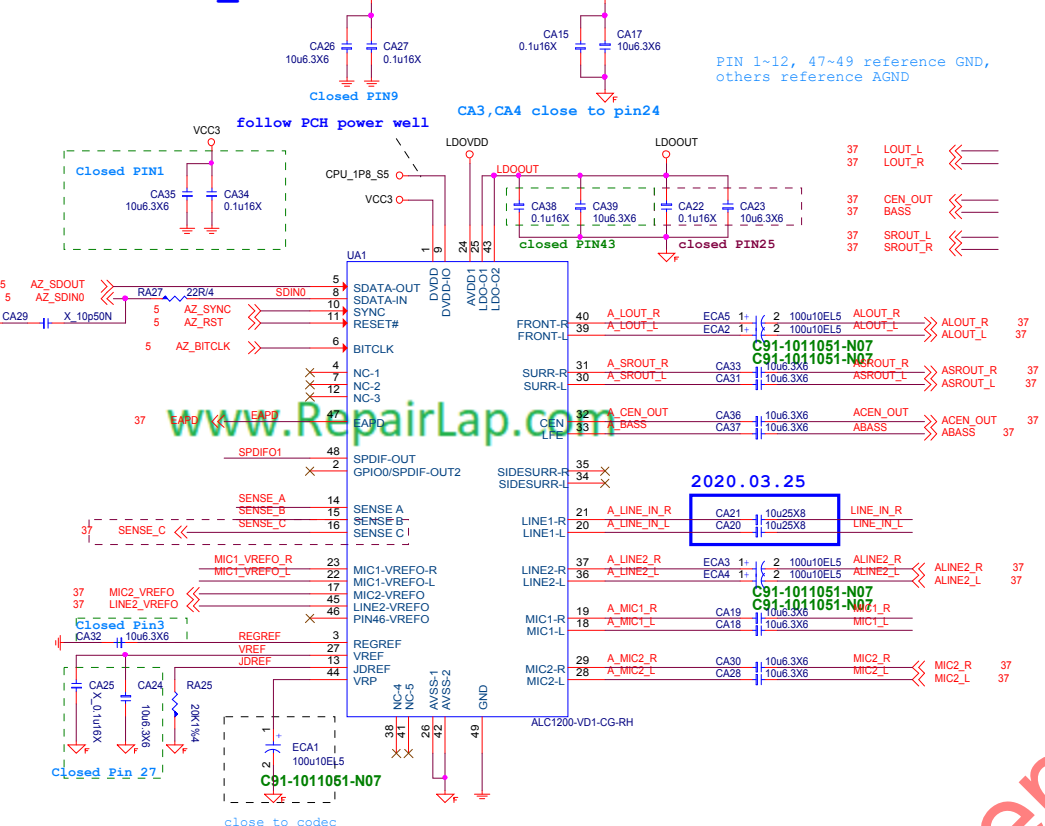


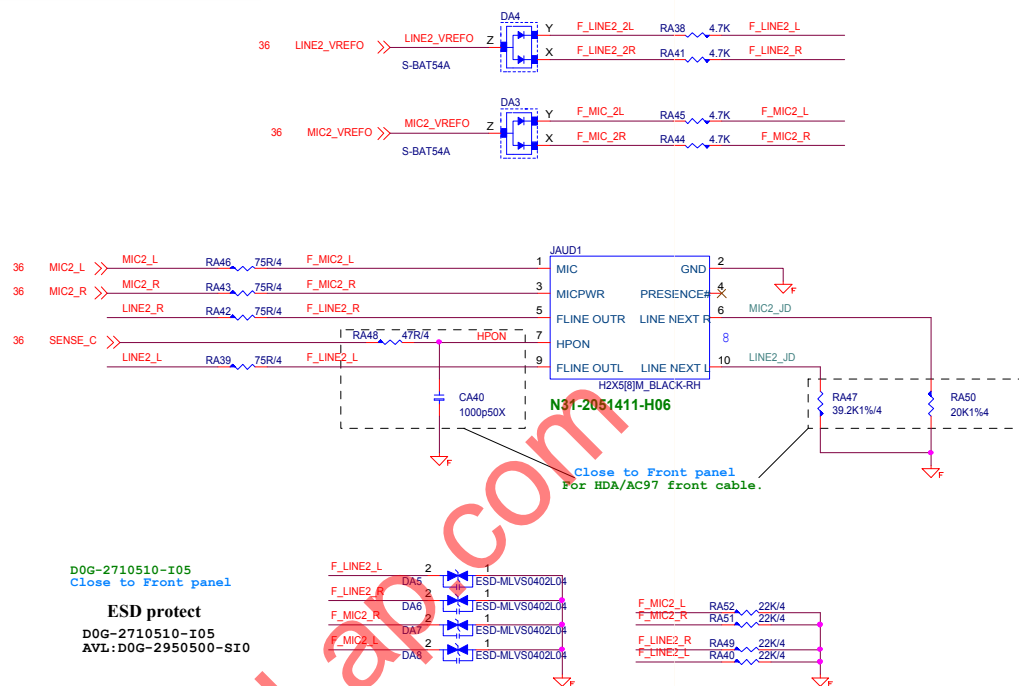
2020.04.07
Removed

3.3V Icc Max:100mA
0.95V Icc Max:650mA

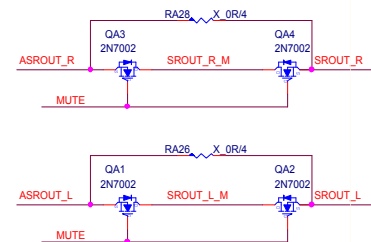
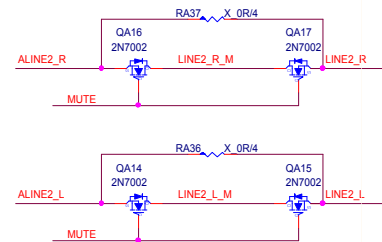
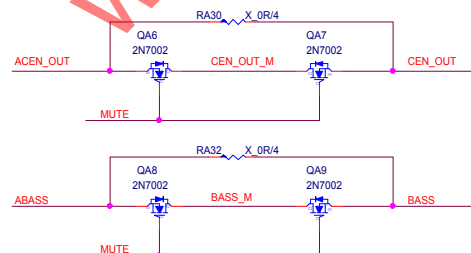
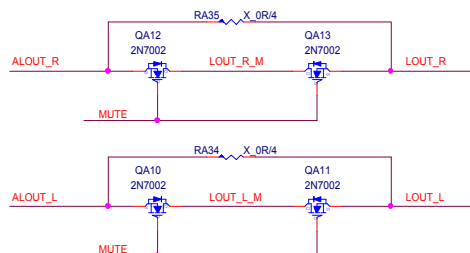
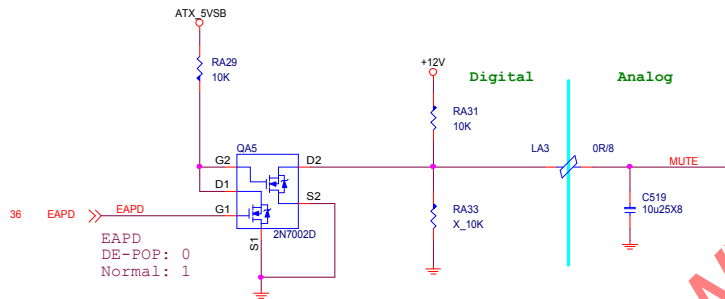
MICRO-STAR INT'L CO.,LTD			
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ALC1200-VD1_48PIN



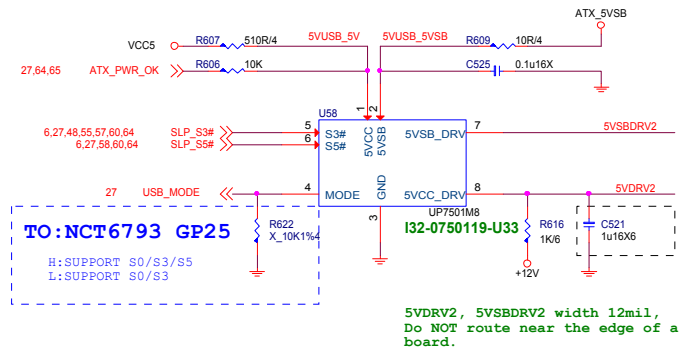


De-POP circuit

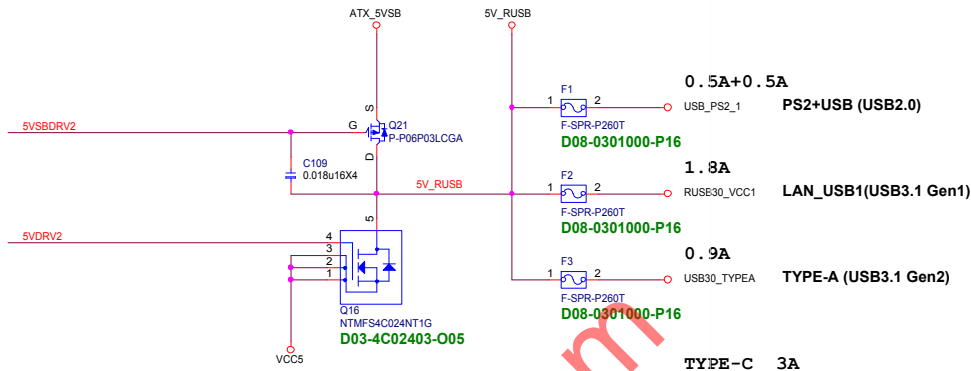


- LOUT_L 36
- LOUT_R 36
- SROUT_L 36
- SROUT_R 36
- CEN_OUT 36
- BASS 36
- ALINE2_R 36
- ALINE2_L 36
- ALOUT_R 36
- ALOUT_L 36
- ASROUT_R 36
- ASROUT_L 36
- ACEN_OUT 36
- ABASS 36

USB Power

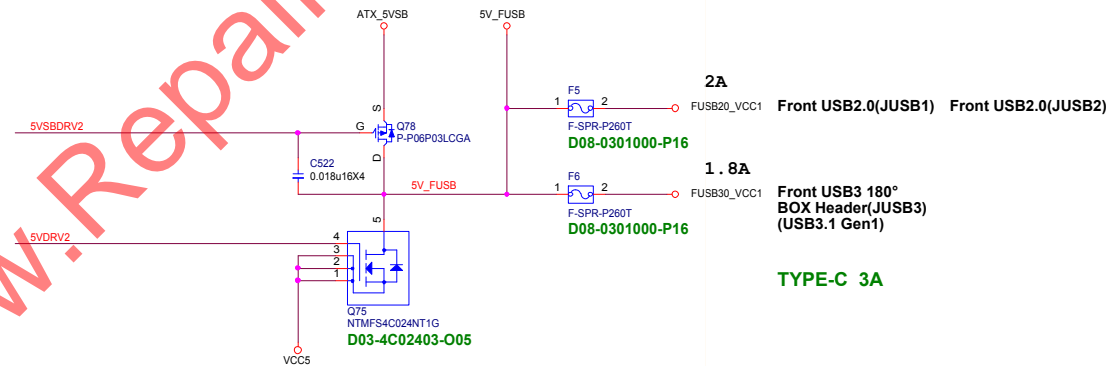


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Rear (6.7A)

Front (6.8A)



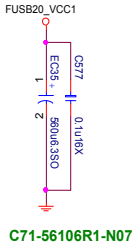
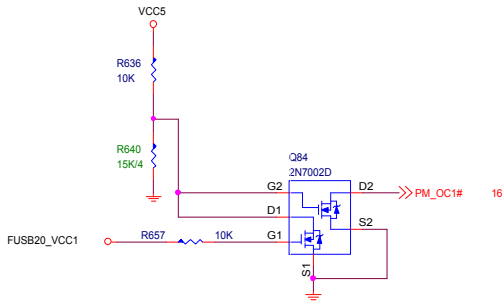
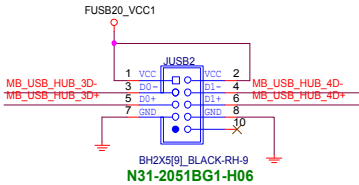
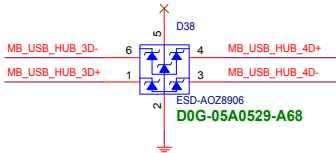
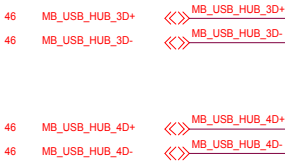
MICRO-STAR INT'L CO.,LTD

MS-7C91

Size	Document Description	Rev
Custom	USB Power - UP7501	10
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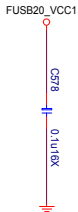
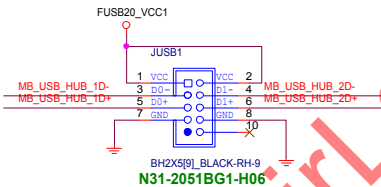
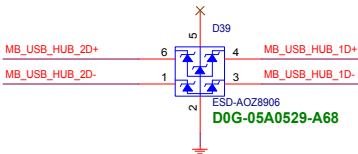
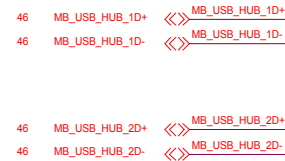
Front USB2.0 (JUSB2) Form GL850G USB2.0 HUB

5V@1A



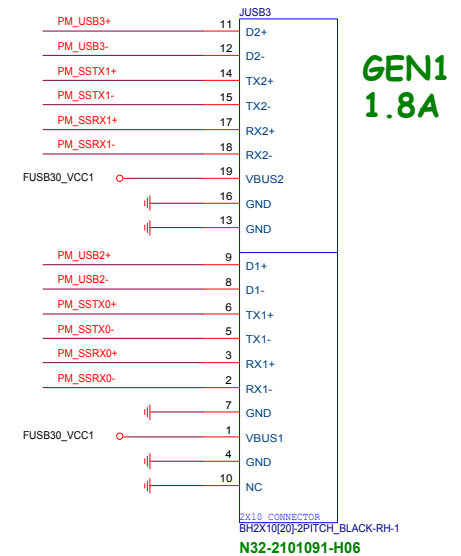
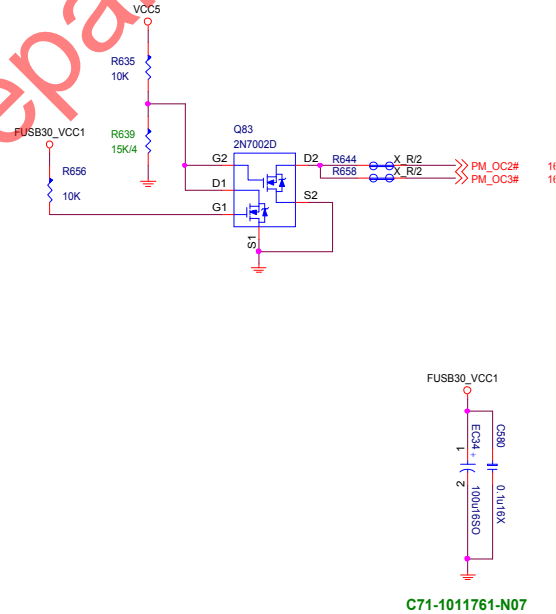
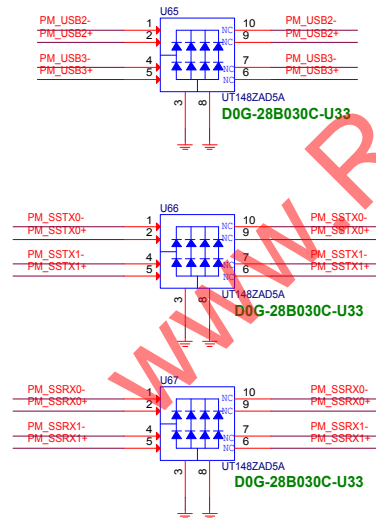
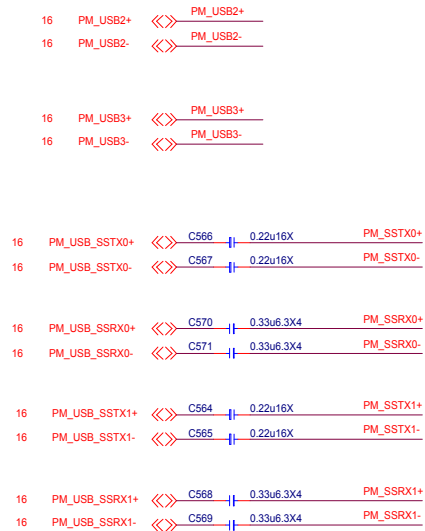
Front USB2.0 (JUSB1) Form GL850G USB2.0 HUB

5V@1A



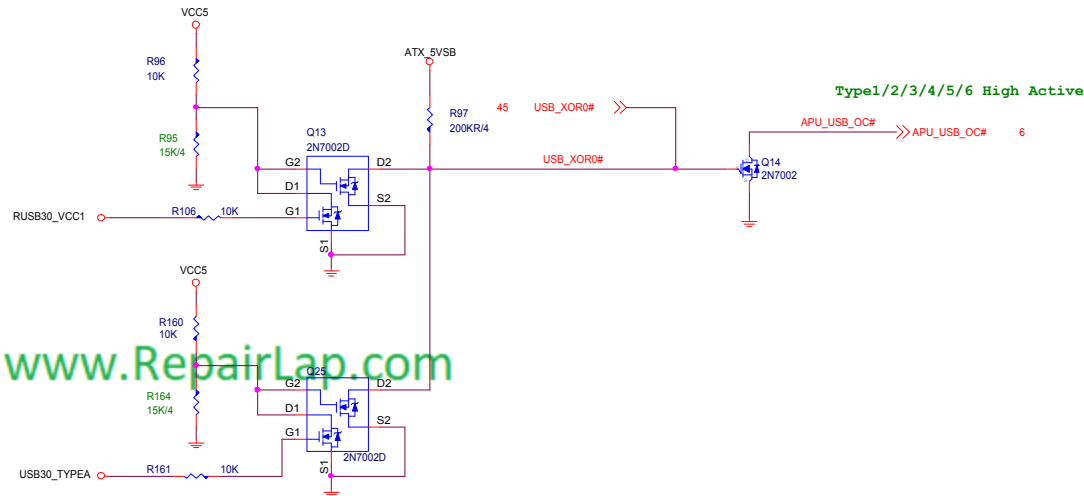
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Front USB3 180°
BOX Header(JUSB3)
5V@1.8A

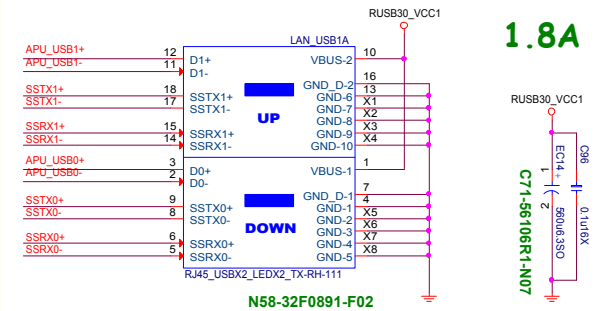
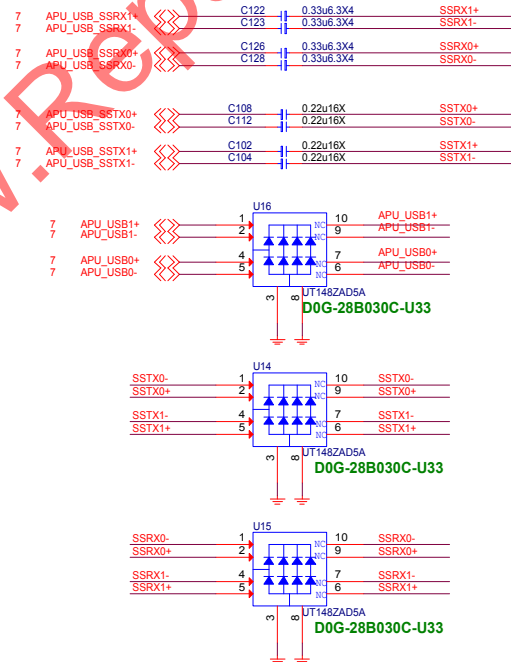


MSI			
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MS-7C91			
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Custom	Front USB3.0 Header		10
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CPU USB_OC

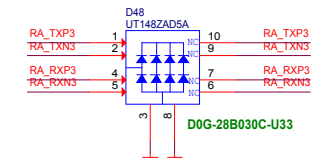
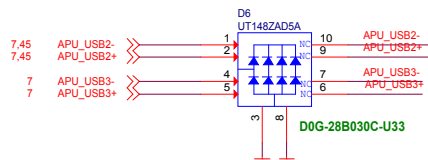
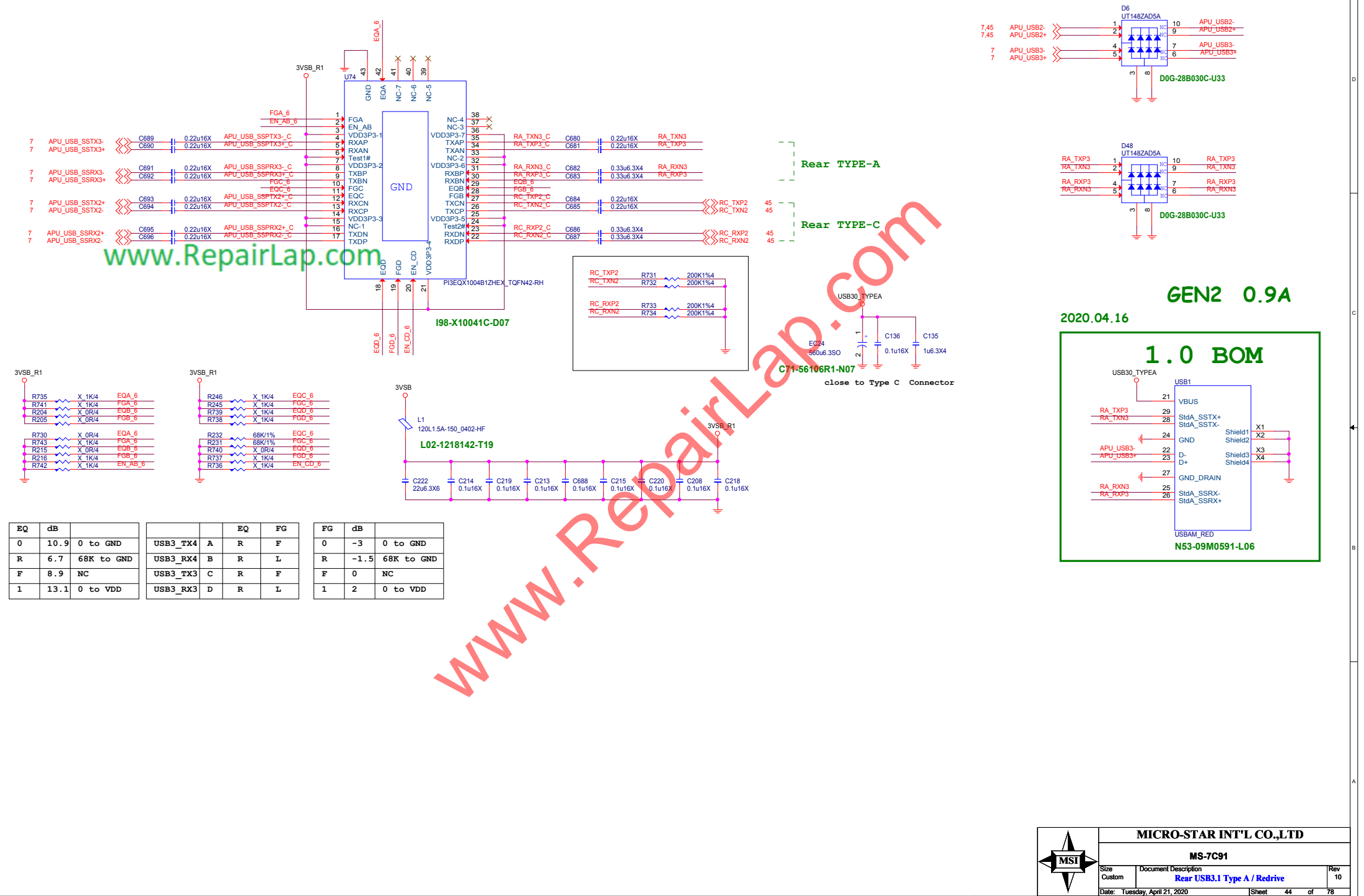


Rear USB3.1 GEN1 5V@1.8A



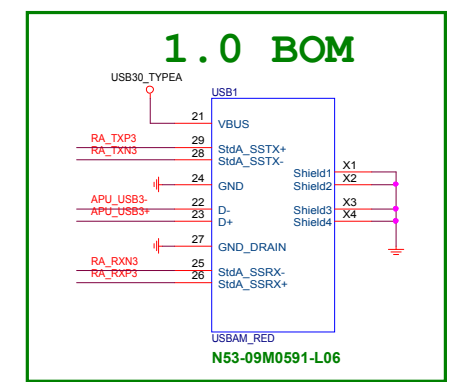
MICRO-STAR INT'L CO.,LTD			
MS-7C91			
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Custom	Rear USB3.1.	10	
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TYPE-A PI3EQX1004 Redriver



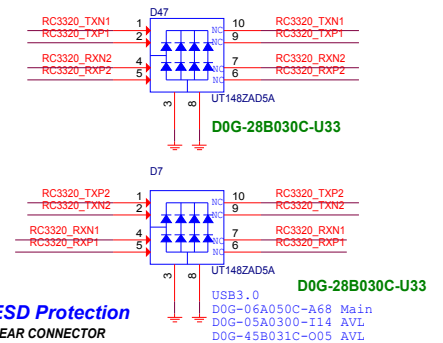
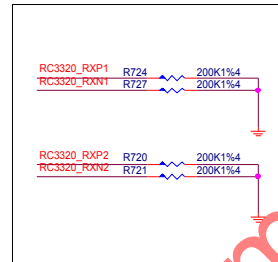
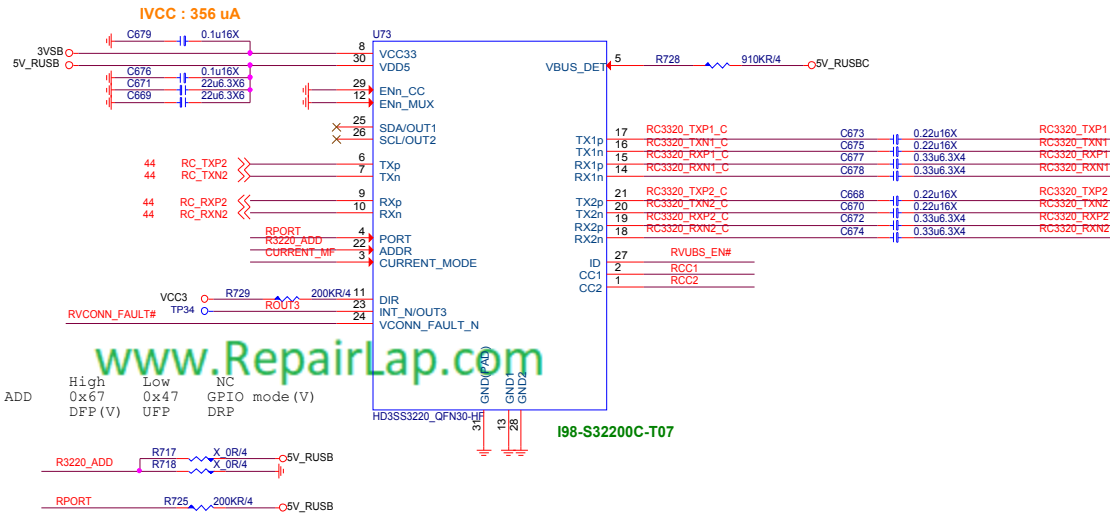
GEN2 0.9A

2020.04.16

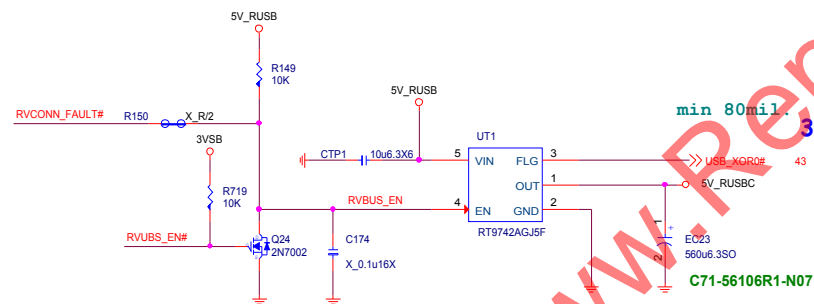


EQ	dB		EQ	FG	FG	dB	
0	10.9	0 to GND	USB3_TX4	A	R	F	
R	6.7	68K to GND	USB3_RX4	B	R	L	
F	8.9	NC	USB3_TX3	C	R	F	
1	13.1	0 to VDD	USB3_RX3	D	R	L	

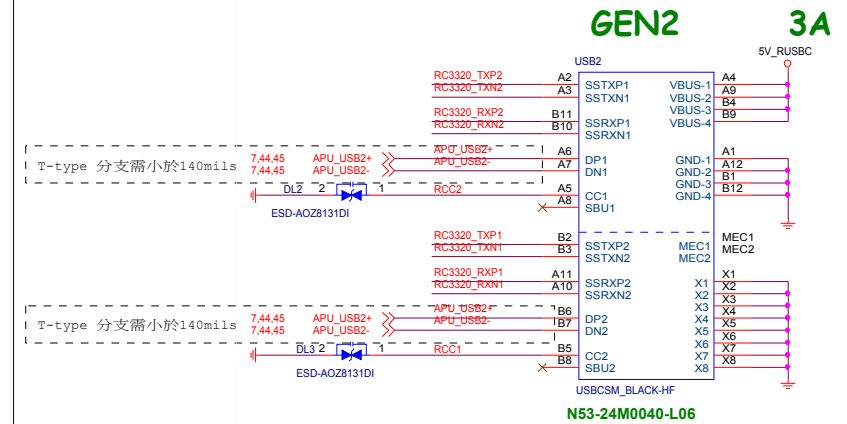
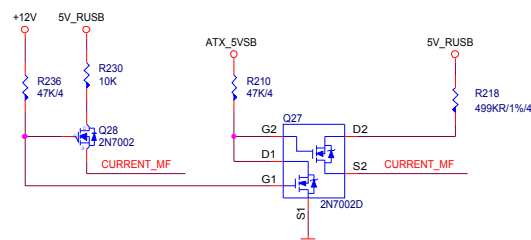
USB 3.1-Type-C USB Type-C MUX with Configuration Channel (CC)



VBUS EN



Current Mode

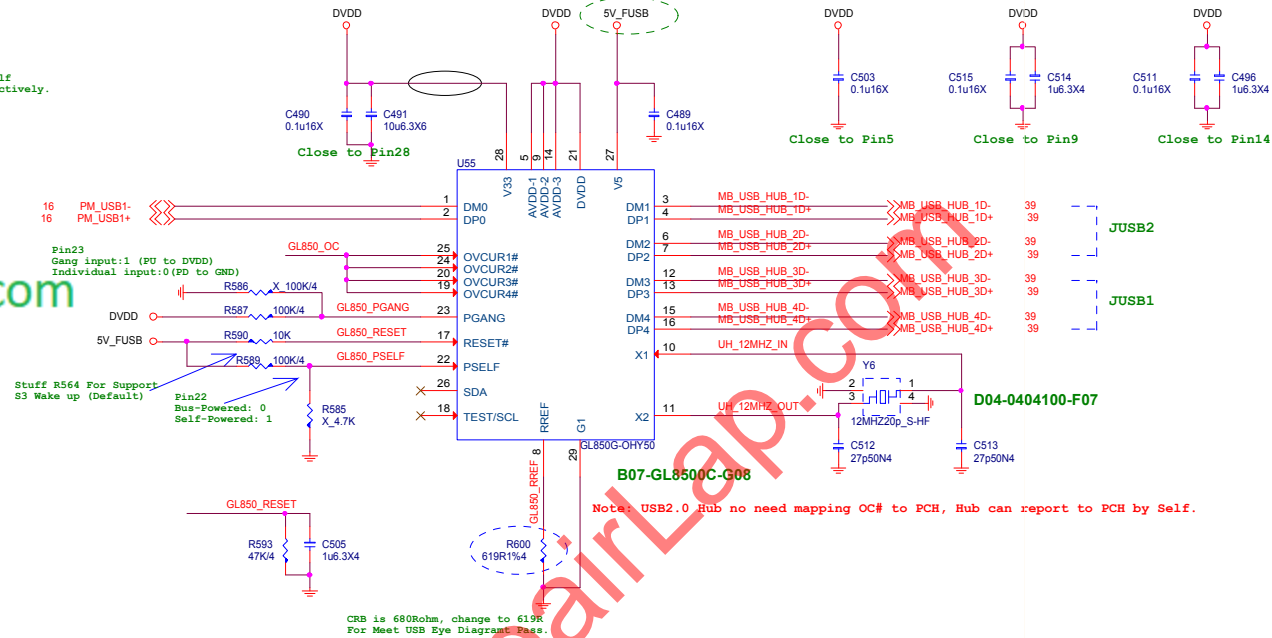


GL850G USB2.0 HUB

5V_FUSB

Note: Not used OC Function For HUB Self
Please connect to OC pin of PCH Respectively.

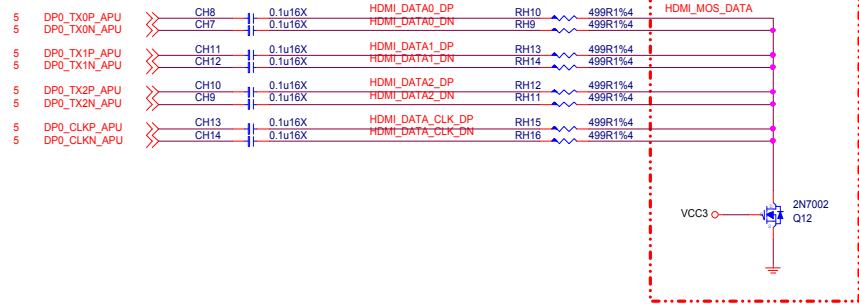
Note: Please connect to USB Power Source.

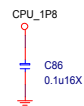


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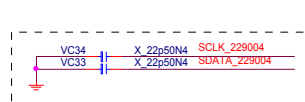
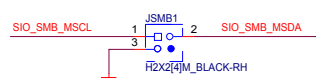
HDMI CONNECTOR

For HDMI 1.4





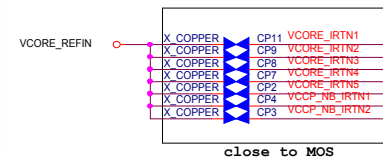
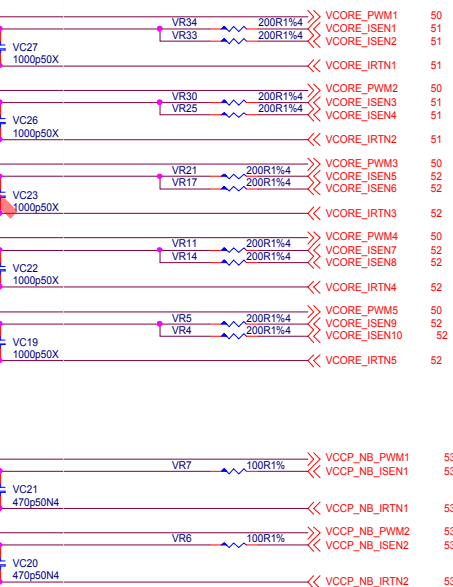
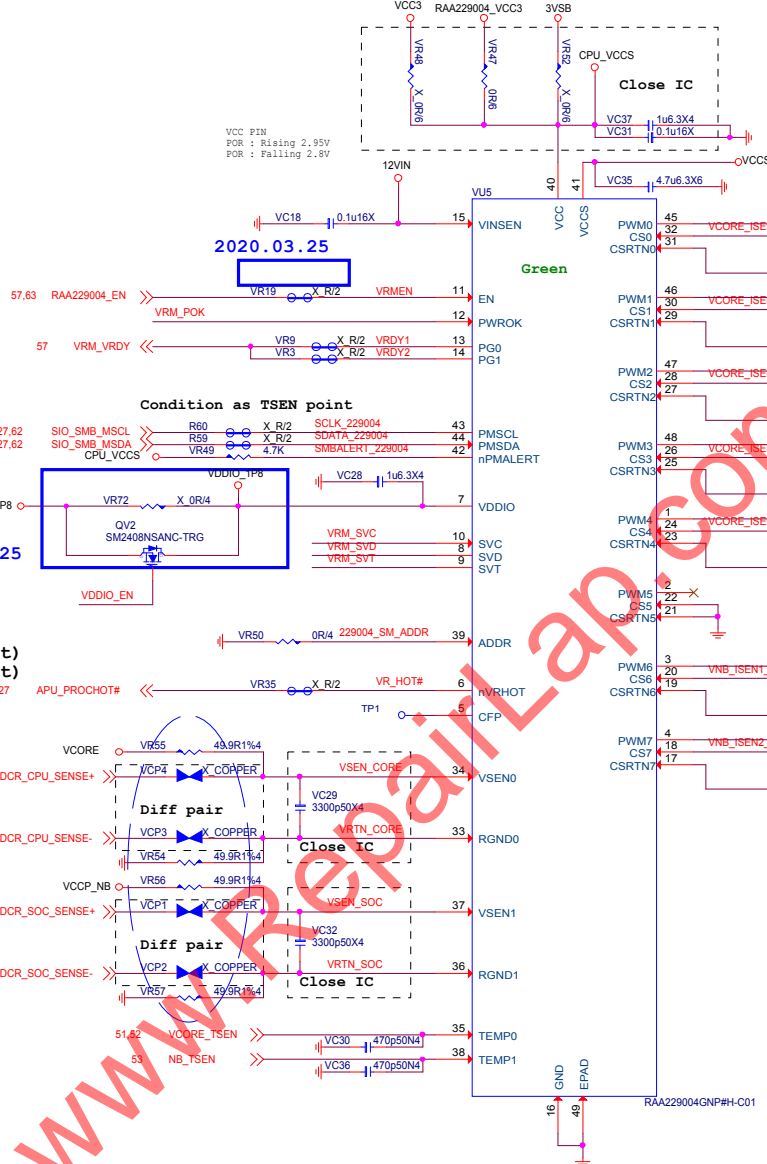
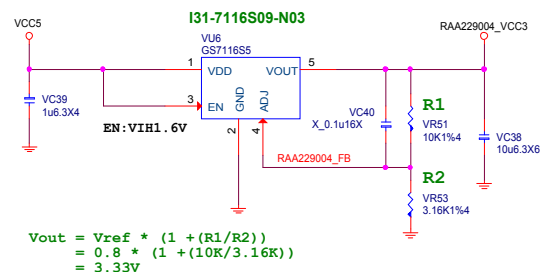
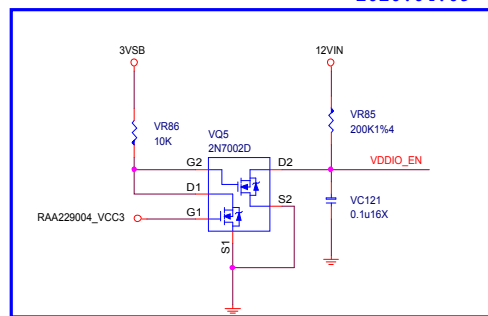
		BOOT VOLTAGE
SVC	SVD	Pre_PWROK Metál VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



```
SMBUS address:0X60 (7 bit)
                0XC0 (8 bit)
```



2020.04.09



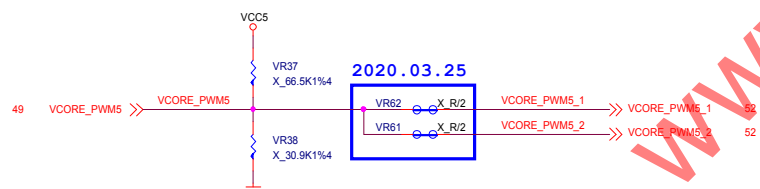
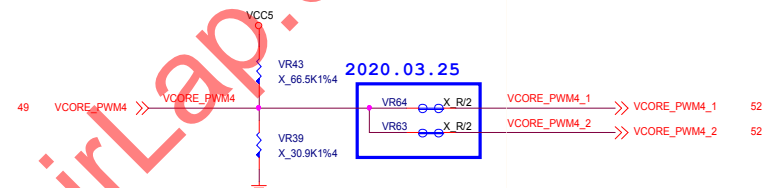
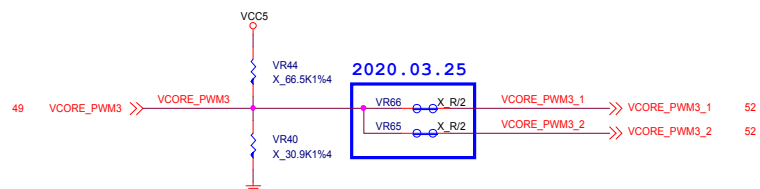
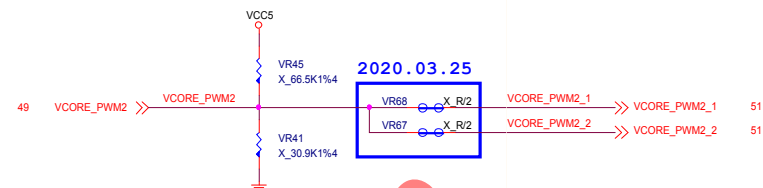
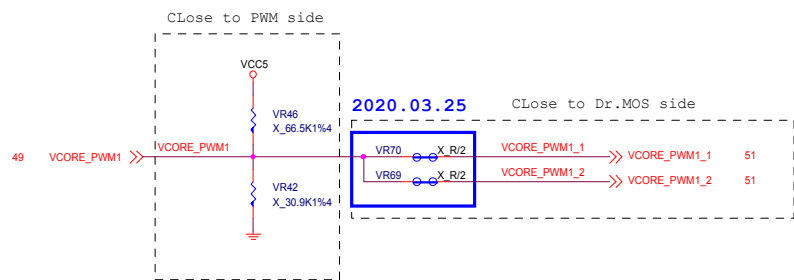
MICRO-STAR INT'L CO.,LTD

MS-7C91

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CPU_CORE Driver IC

VCORE Double 10-PHASE

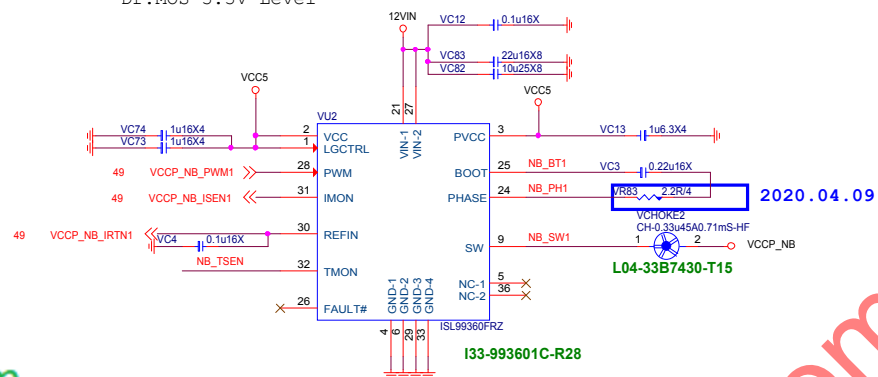


MICRO-STAR INT'L CO.,LTD

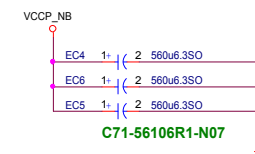
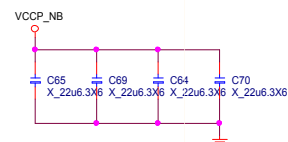
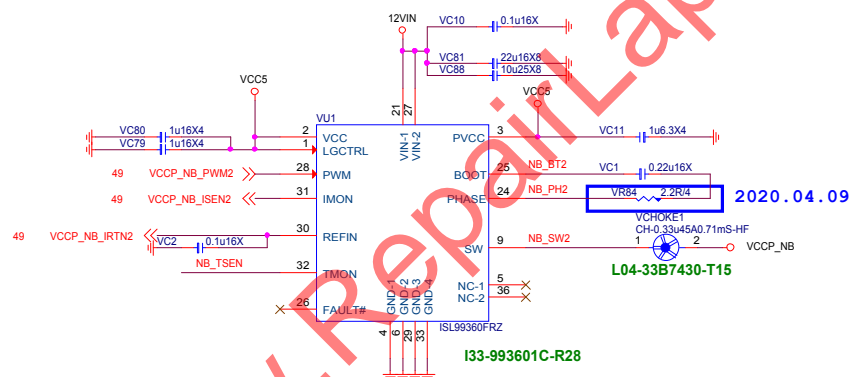
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Dr.MOS 3.3V Level



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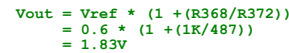
Size	Document Description	Rev
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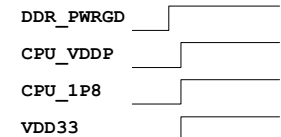
www.RepairLap.com

 MSI <small>Micro-Star International</small> <i>Link to the Future</i>			MICRO-START INTL CO.,LTD.		
Title CPU Power NB Switch / NCT3933 OV					
Size	Document Number				Rev
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CPU 1.8V_S5@0.5A
CPU_VDDP_S5@1A
AUDIO1.8V@0.25A

$$I_{\max} = 3.75A(S_5 + S_0)$$


CPU 1.8V_S0@2A



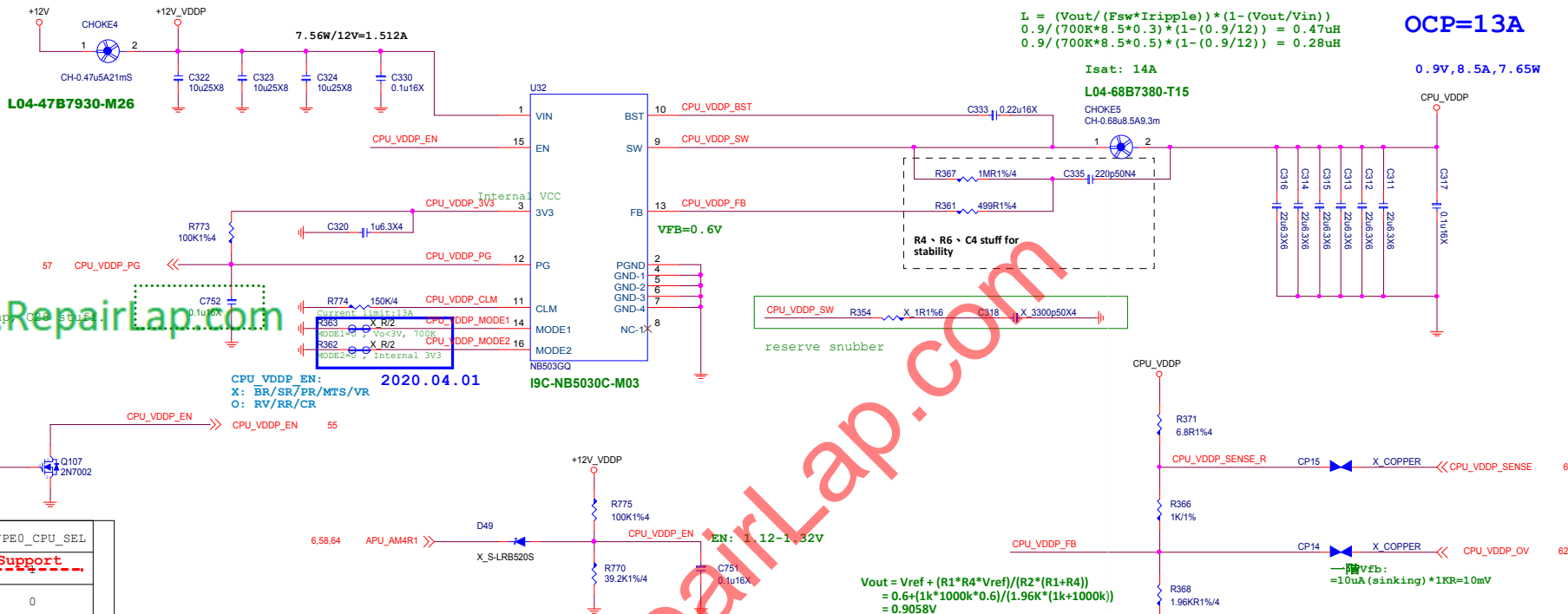
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Size Custom	Document Description CPU Power 1.8_S0 / S5	Rev 10
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CPU_VDDP_S0

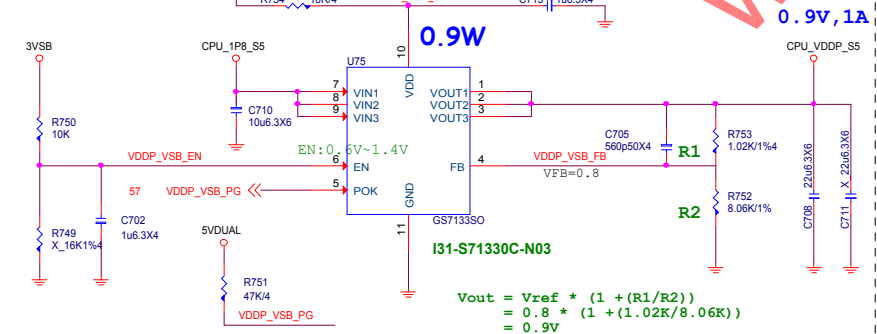
0.9V@S0:8.5A

Input Current = $(13A \cdot 0.9V) / 12V / 0.8 = 1.22A$
 Choke Isat = 8A
 $I_{rms} = I_{out} \cdot \sqrt{((V_o/V_i) \cdot (1 - (V_o/V_i)))}$
 $= 13 \cdot \sqrt{((0.9/12) \cdot (1 - (0.9/12)))} = 3.42A$
 Choke I_{rms} = 5A



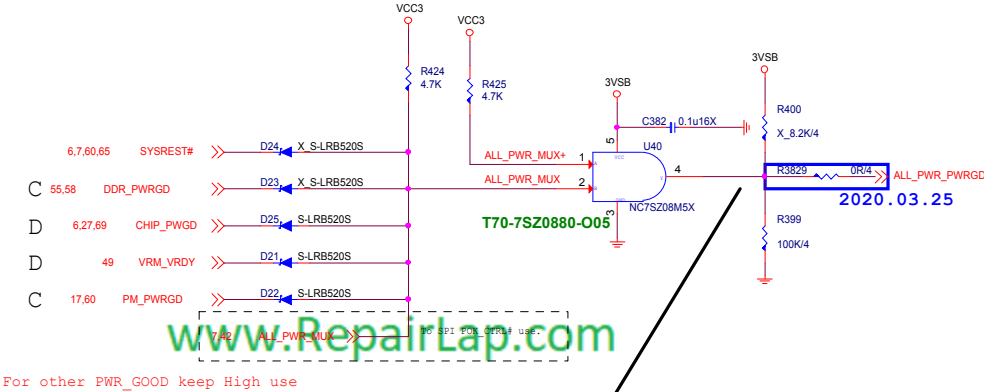
CPU_VDDP_S5

0.9V
S5:1A



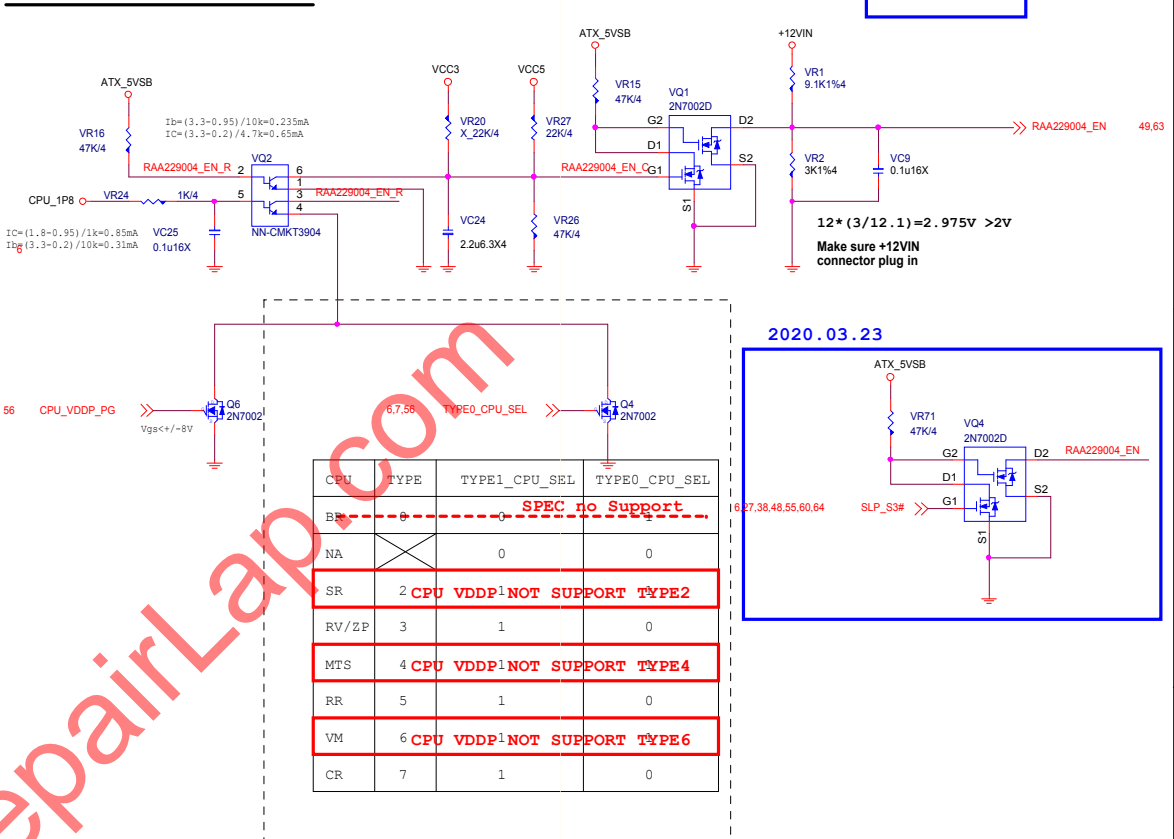
ALL POWER GOOD MUX

S0 PG

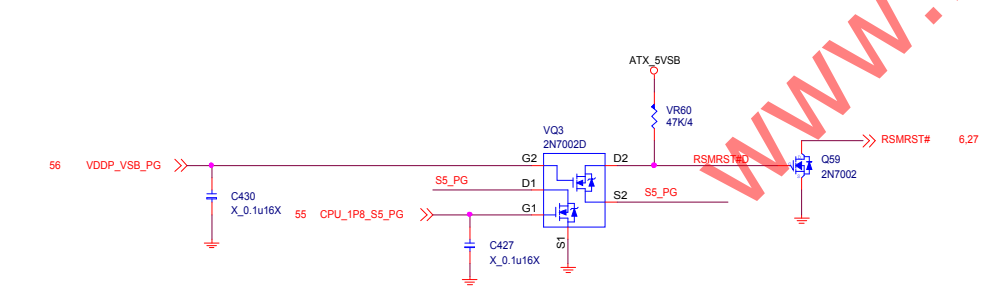


When you use external buffer then you cannot let APU PWR_GOOD pin float in any sleep state. If you're buffer use 3.3V_S0 and you need Pull-down 100K. If you're buffer use 3.3V_S5 and you don't need PD.

VRM_Enable circuit



S5 PG



DDR4_1.2V@28.7A

18A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

$$\begin{aligned} \text{Rocset} &= 1.5 * \text{Imax} * \text{Rdson}(\text{Low side}) / \text{Iocset} \\ &= 1.5 * 28.7\text{A} * 2\text{mohm} / 10\text{uA} \\ &= 8.61\text{K} \end{aligned}$$

OCP = 43.05A; Choke Isat=43A

$$\begin{aligned} \text{Rocset} &= 1.5 * \text{Imax} * \text{Rdson}(\text{low}) / \text{Iocset} \\ \text{R639} &= 1.5 * 28.7 * 2\text{mohm} / 10\text{uA} \\ \text{R639} &= 8.61\text{K} \end{aligned}$$

Rdson(Low Side) 5V
D03-4C02403-005:3.3 ~ 4mohm

$$\begin{aligned} 10\text{mV} * (1.96\text{K} / 2.96\text{K}) &= 6.62\text{mV} \\ \text{REFIN}(\text{R625}) &= 6.62\text{mV} / 10\text{uA} = 662\text{R} \end{aligned}$$

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DDR VR EN
FROM SIO_VDDQ_EN:R230/R220 stuff
FROM VPP_VR_PG:R230/R220 un stuff

Default:FCCM
L:FCCM
H:DEM

Default:FCCM
4.5V:FCCM
2.37V:DEM

$$\begin{aligned} \text{Rocset} &= 1.5 * \text{Imax} * \text{Rdson}(\text{Low side}) / \text{Iocset} \\ &= 1.5 * 28.7\text{A} * 2\text{mohm} / 10\text{uA} \\ &= 8.61\text{K} \end{aligned}$$

$$\text{Input Current} = (28.7 * 1.2) / 5 / 0.8 = 8.61\text{A}$$

L04-68B7350-T15

CH0-0.68u15A5mS

C71-56106R1-N07

2020.03.31

L04-47B71F0-T15

CH0-0.47u35A0.88m

C71-56106R1-N07

C71-56106R1-N07



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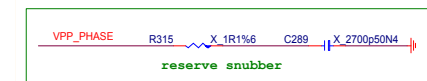
MS-7C91

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2.5V@2.24A



VPP_BST>50 mils.



To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

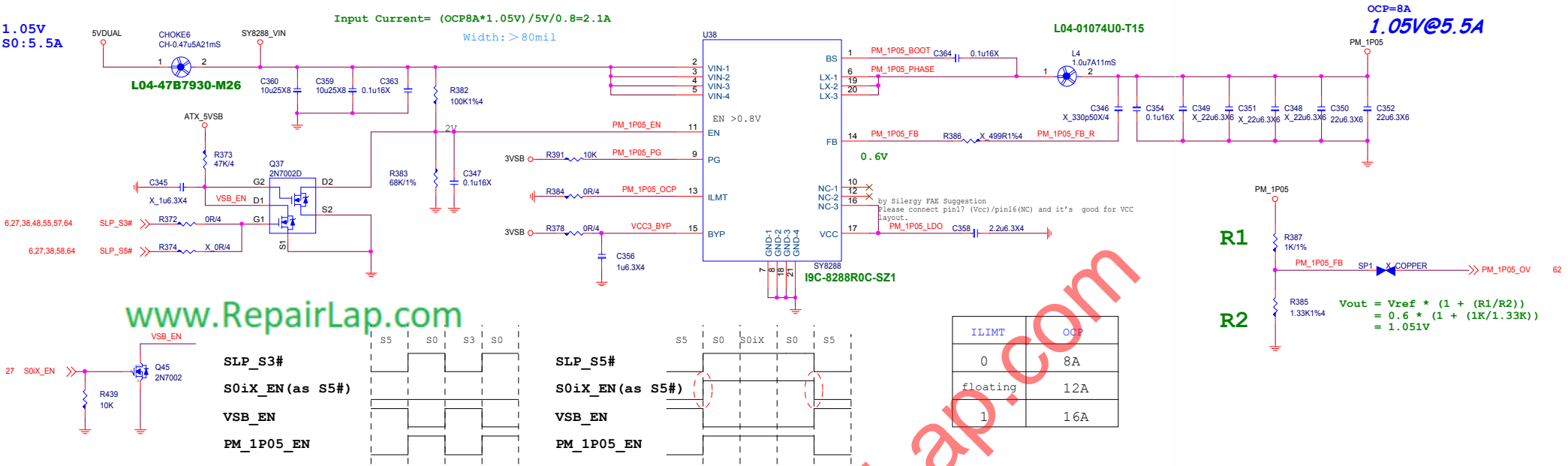


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Size Custom	Document Description DDR VPP25 / VTT	Rev 10
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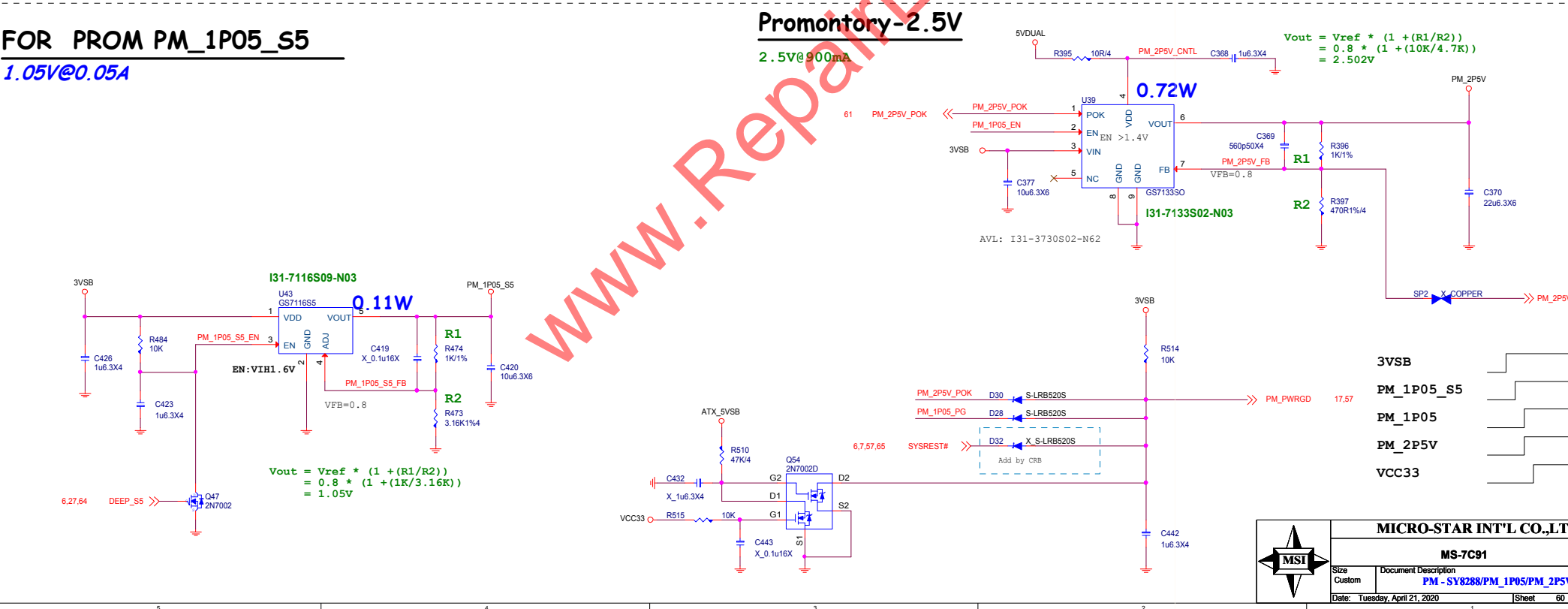
FOR Promontory 1.05V_S0

1.05V
S0:5.5A



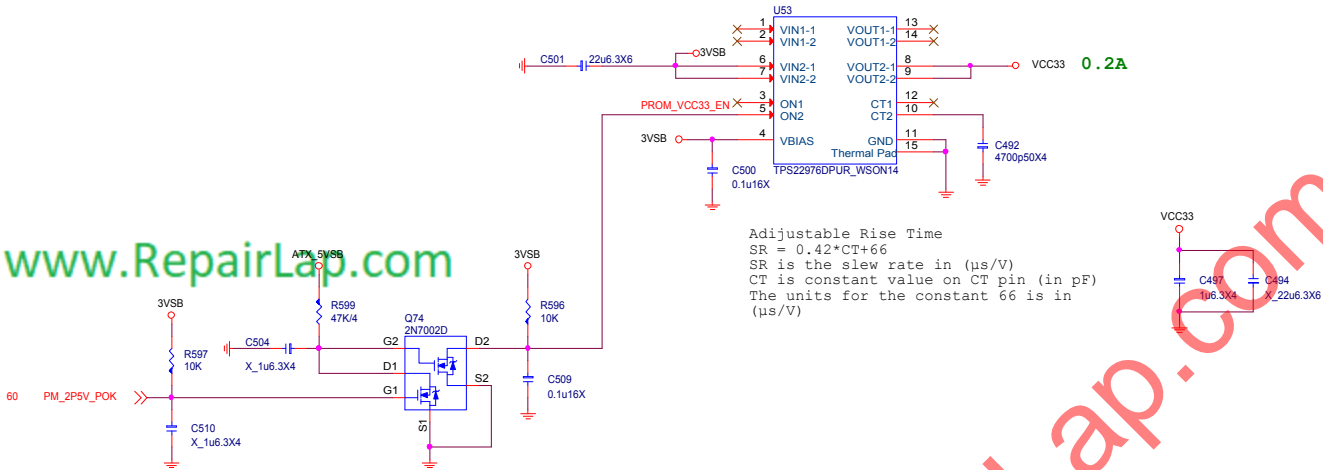
FOR PROM PM_1P05_S5

1.05V@0.05A



PROM VCC33

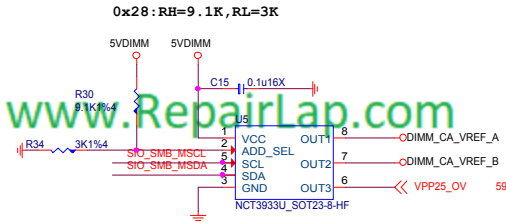
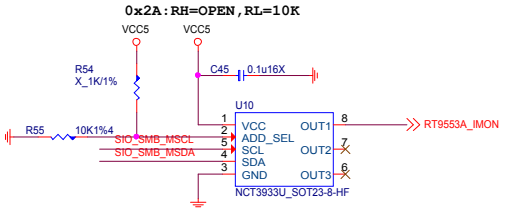
VCC33@0.2A



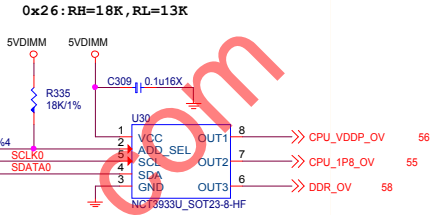
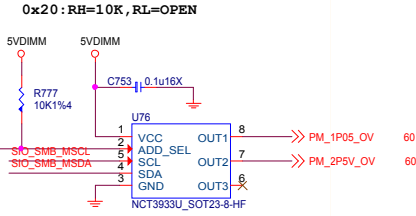
Over Voltage Control IC

UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



6.27.49 SIO_SMB_MSC_L SIO_SMB_MSC_L
6.27.49 SIO_SMB_MSDA SIO_SMB_MSDA



6.11.24 SCLK0 SCLK0
6.11.24 SDATA0 SDATA0

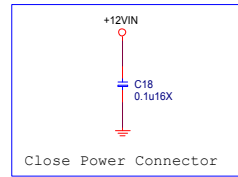
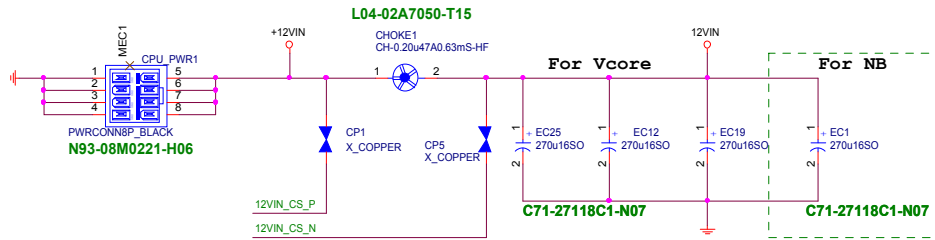


MICRO-STAR INT'L CO.,LTD

MS-7C91

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CPU POWER CONNECTOR



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$$\Delta V_{ILIM} = 10\mu A * [(60.4K * 40.2K) / (60.4K + 40.2K)] = 226mV$$

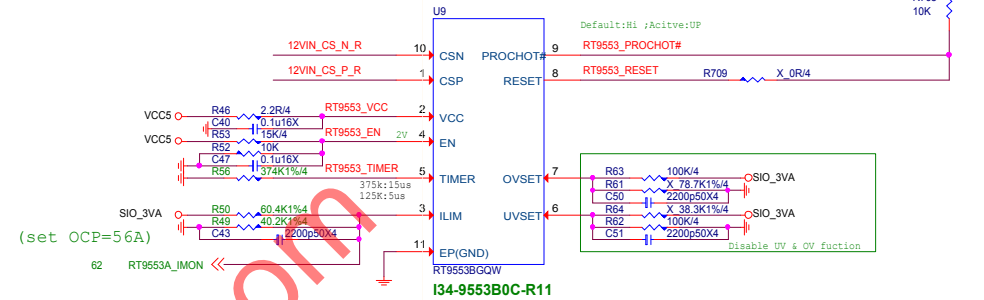
$$I_{sense} = V_{ILIM} / 100 * R_{sense}$$

$$\Delta I_{sense} = 226mV / 100 * 0.63m = 3.58A$$

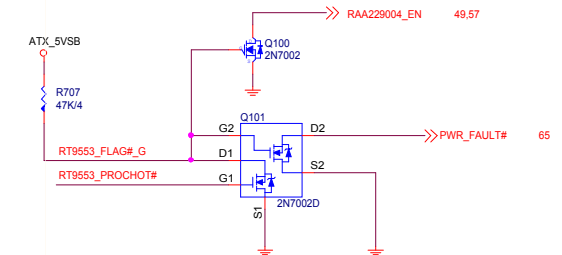
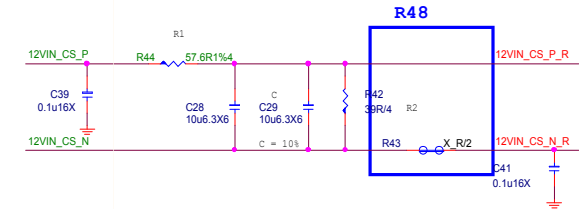
Vcore		SOC	
D=Vout/Vin		D=Vout/Vin	
Vin = 12	> input voltage	Vin = 12	> input voltage
Vout = 2	> output Vcore	Vout = 1.55	> output Vcore
D = 0.16667		D = 0.129167	
I_o = Icore(max)*0.8		I_o = Icore(max)*0.8	
I core(max) = 200	> Vcore current	I core(max) = 75	> Vcore current
I avg. = 160	A	I avg. = 60	A
I ripple={ I_o*√D*√(1-D) } / Phase		I ripple={ I_o*√D*√(1-D) } / Phase	
Phase = 10	phase	Phase = 2	phase
I ripple = 5.962848	A	I ripple = 10.06153	A
How many pcs. Of Cap.		How many pcs. Of Cap.	
I ripple(cap) = 4700	m A	I ripple(cap) = 4700	m A
COE _{TEMP} = 1		COE _{TEMP} = 1	
Input Cap. = 2	pcs.	Input Cap. = 3	pcs.

RT9553B CURRENT SENSE

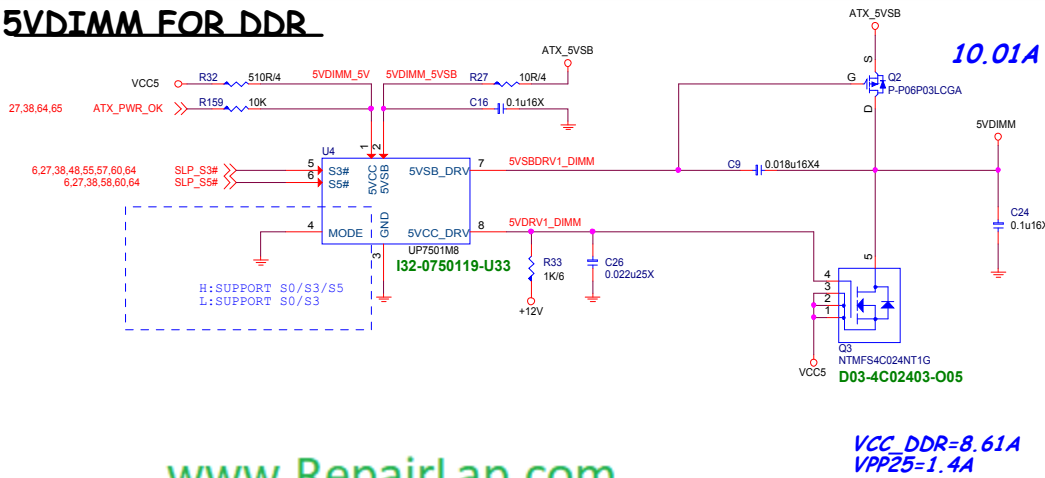
RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.



2020.03.25

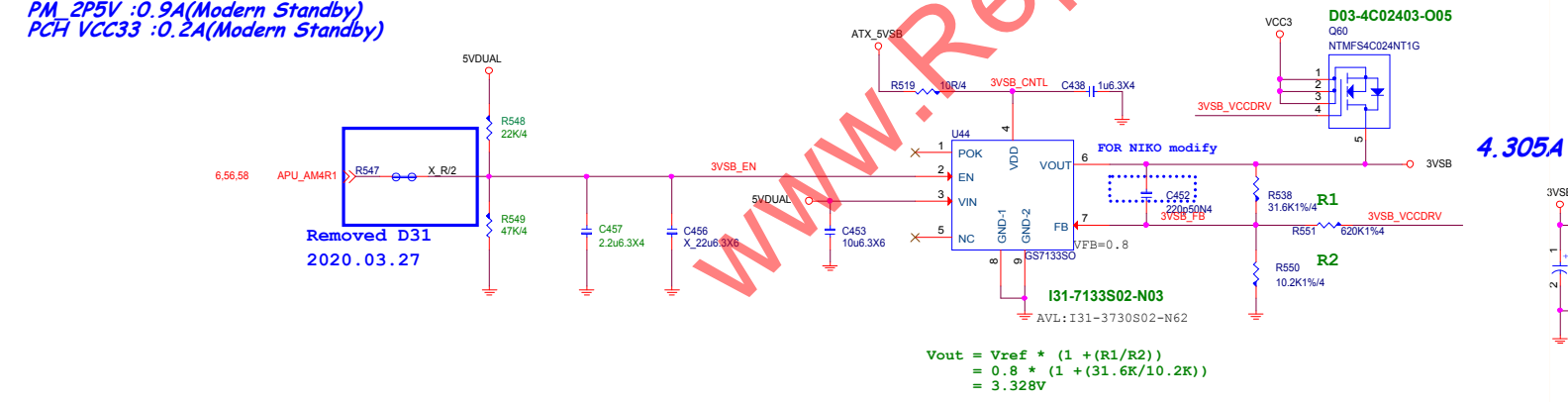


5VDIMM FOR DDR

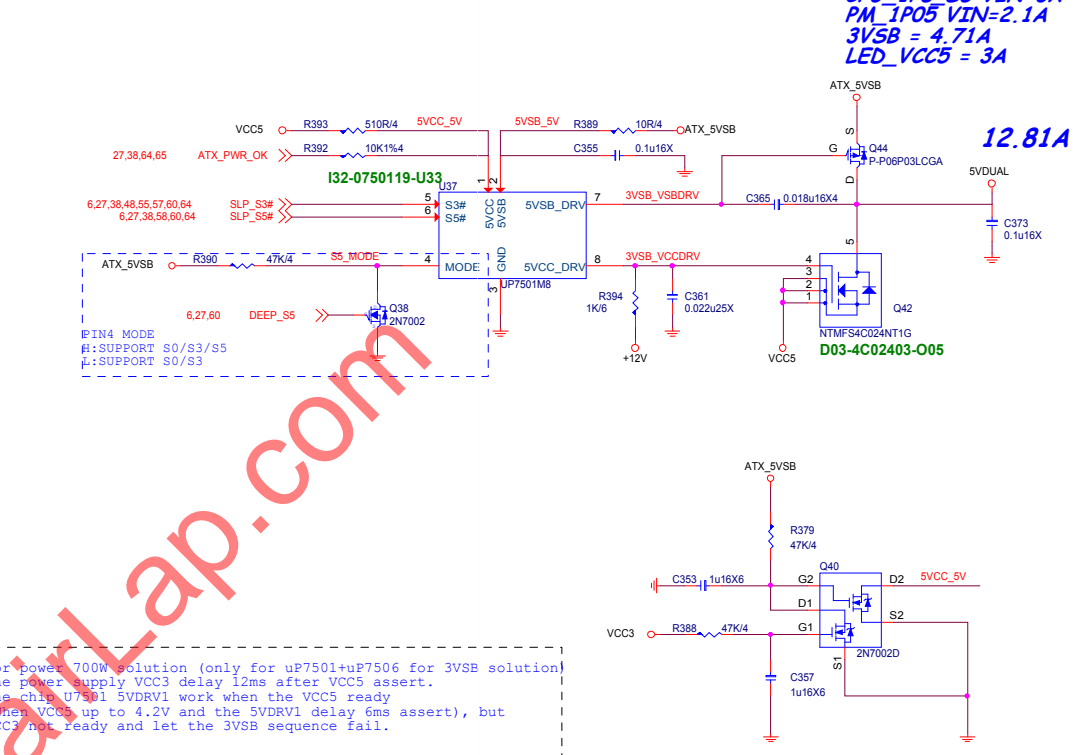


3VSB cost down
3.3V@4.305A

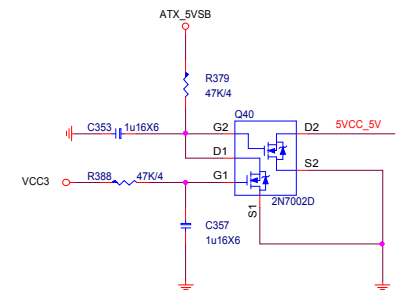
CPU:VDD_33_S5=0.25A
CHIP:VDD_33_S5=0.07A
PCIE=(375mA*5)=1.875A
M.2WIFI= 0.78A
RT8111H LAN=0.18A
PM_1P05_S5 :0.05A
PM_2P5V :0.9A(Modern Standby)
PCH VCC33 :0.2A(Modern Standby)



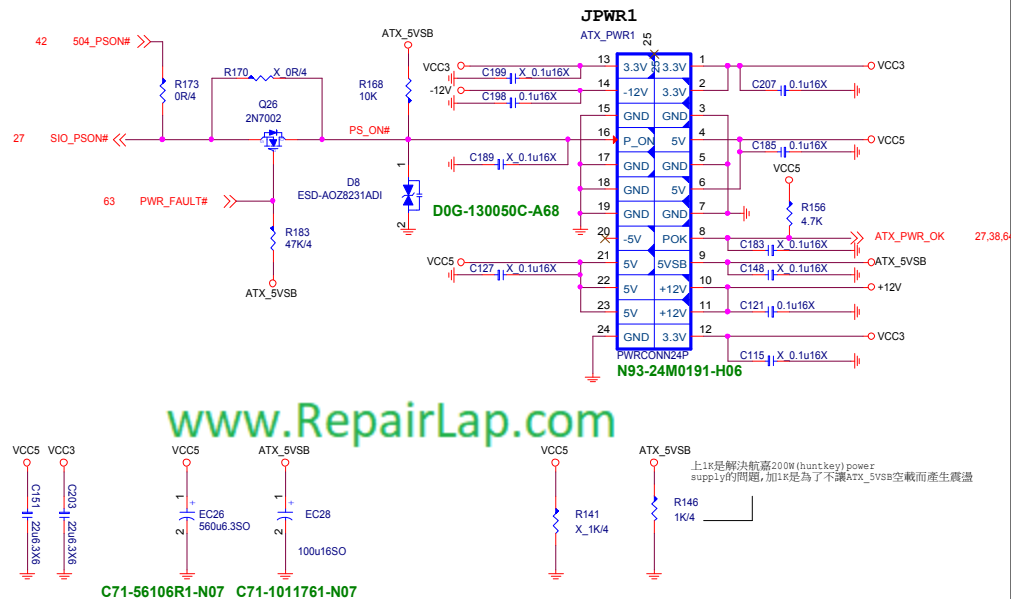
5VDUAL For 3VSB/CPU1.8V/VDDP



For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(when VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

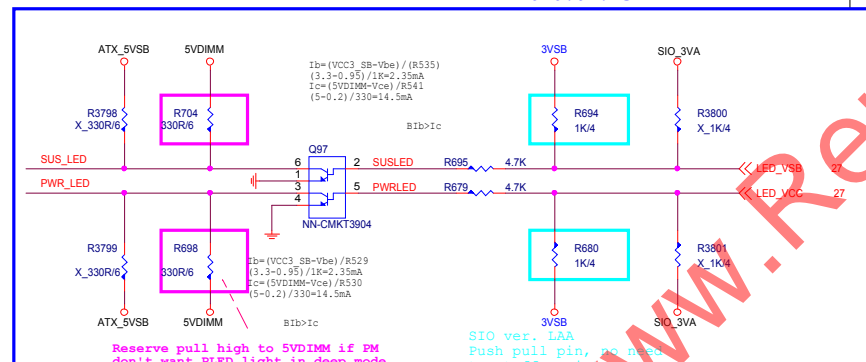


ATX POWER CONNECTOR

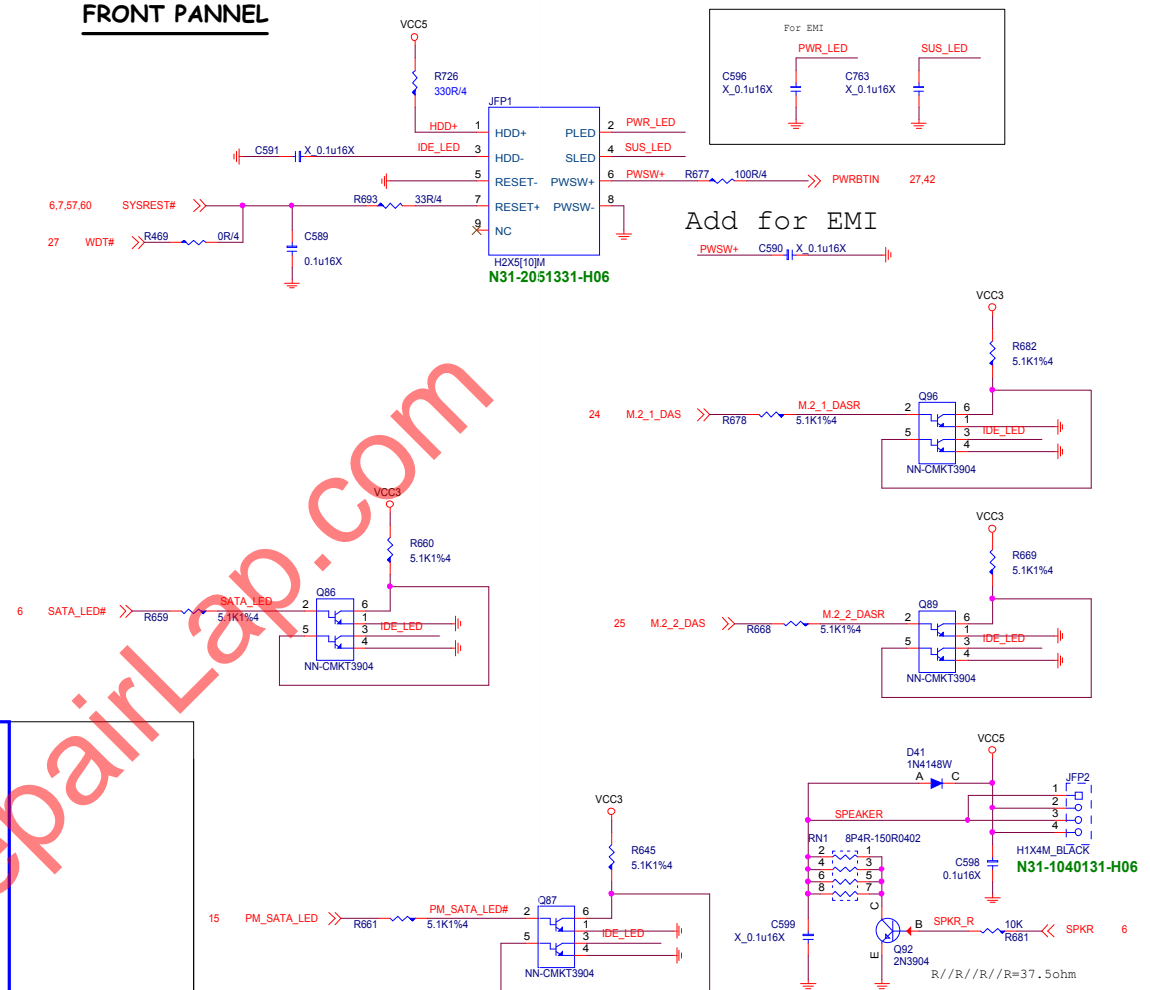


LED (for NCT6687D-R)

2020.04.13



FRONT PANNEL



Voltage Mearsure Point

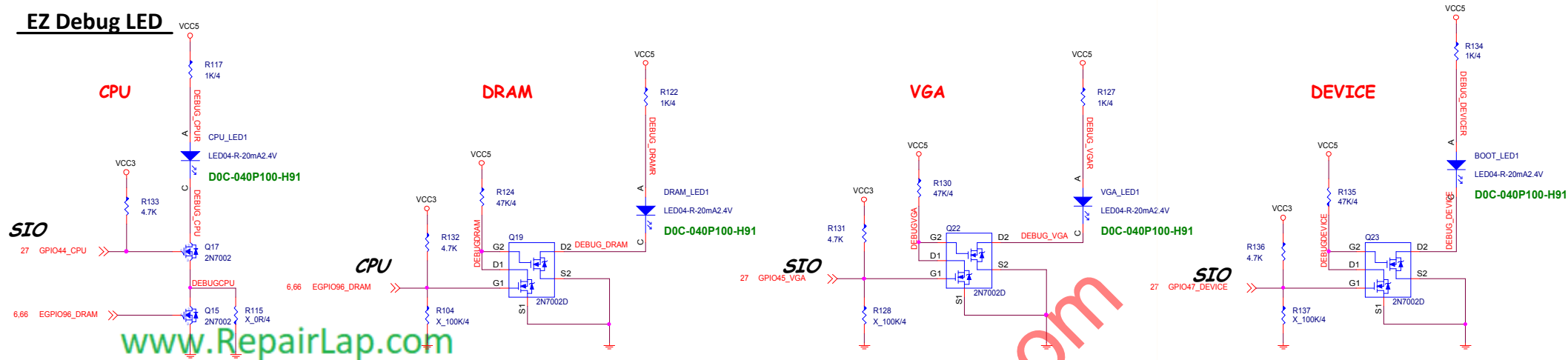


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Size Custom	Document Description ATX power - FrontPanel / EMI	Rev 10
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EZ Debug LED



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LED GPIO	GPIO44	EGPI06	GPIO45	GPIO47
亮	OPEN-Drain	GPO LOW	GPO LOW	GPO LOW
滅	GPO LOW	GPO HIGH	OPEN-Drain	OPEN-Drain

default Input

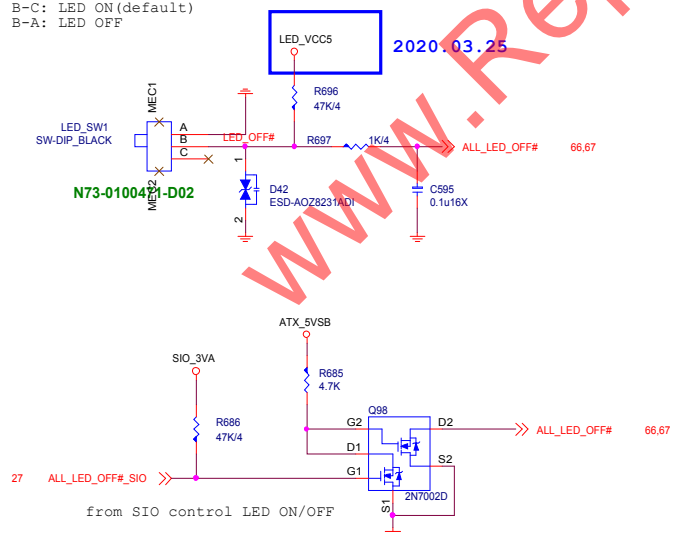
LED亮燈時同時將CPU LED關掉

LED_SW1 FORM SIO

D0C-040P100-H91/D0C-040S500-E07

LED_SW1 for ALL LED OFF

B-C: LED ON(default)
B-A: LED OFF



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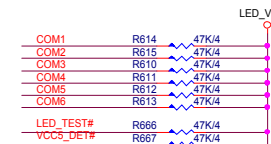
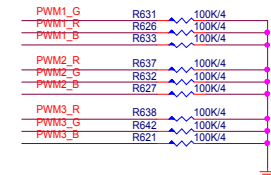
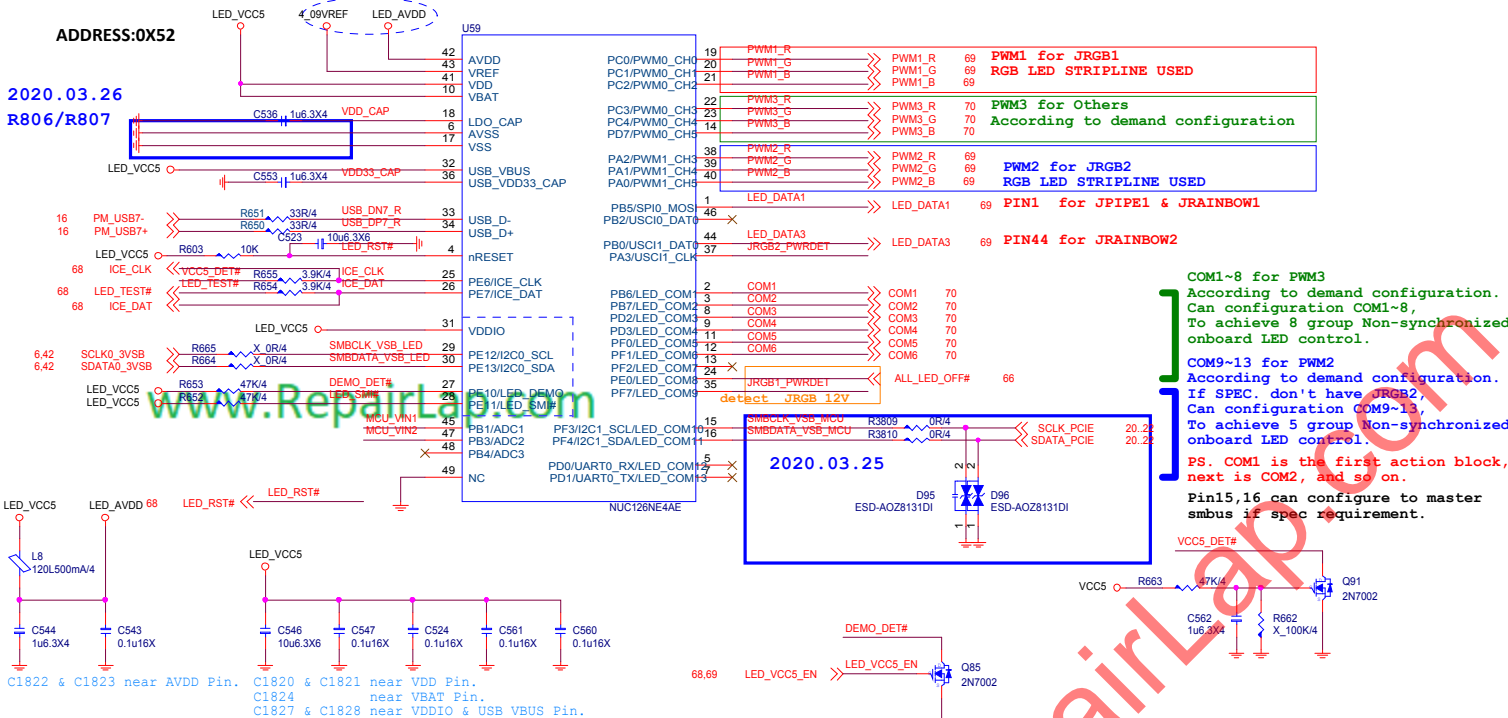
Size	Document Description	Rev
Custom	LED - EZ DEBUG / AMP	10
Date: Tuesday, April 21, 2020	Sheet 66 of 78	

48 PIN LED MCU

If you use ADC function, need to separate VREF from AVDD and 4_09VREF stuff for VREF.

ADDRESS:0X52

2020.03.26
R806/R807

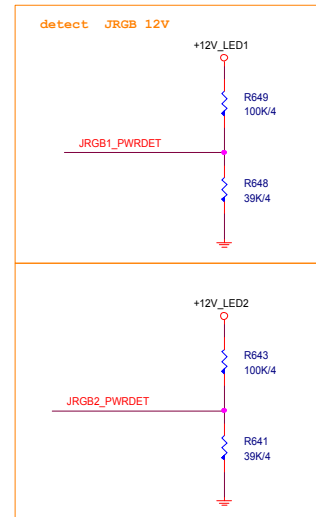


COM1~8 for PWM3
According to demand configuration.
Can configuration COM1~8,
To achieve 8 group Non-synchronized
onboard LED control.

COM9~13 for PWM2
According to demand configuration.
If SPEC. don't have JRGB2,
Can configuration COM9~13,
To achieve 5 group Non-synchronized
onboard LED control.

PS. COM1 is the first action block,
next is COM2, and so on.

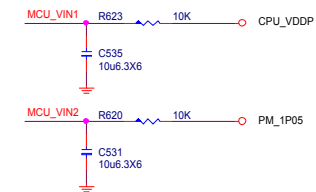
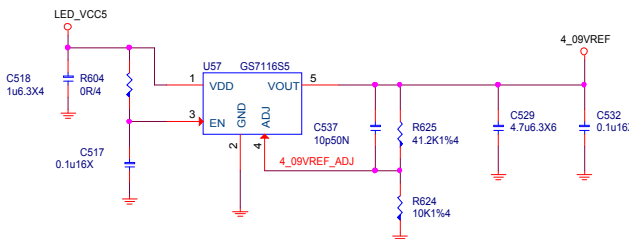
Pin15,16 can configure to master
smbus if spec requirement.



Clear MCU Circuit

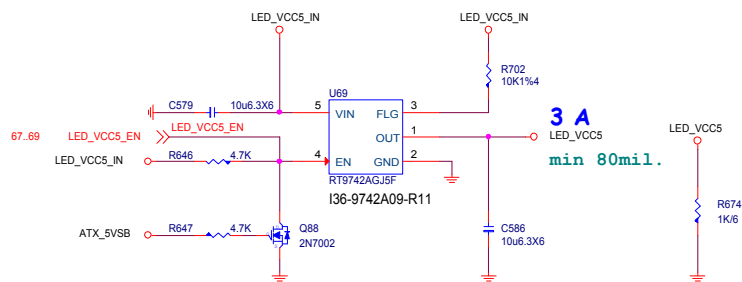


Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

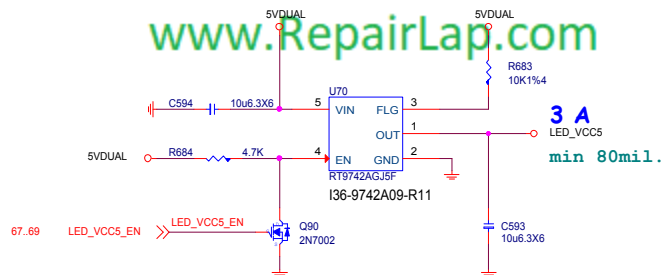


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MS-7C91		
Size	Document Description	Rev
Custom	MCU - LED Control	10
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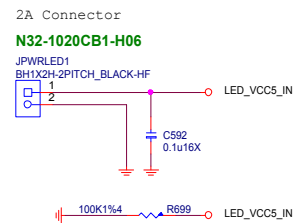
EXTERNAL POWER INPUT



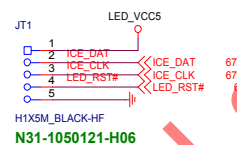
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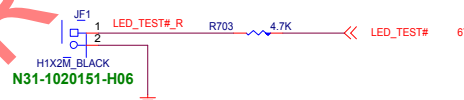
External Power



JT1 for FW update



JF1 for Factory test

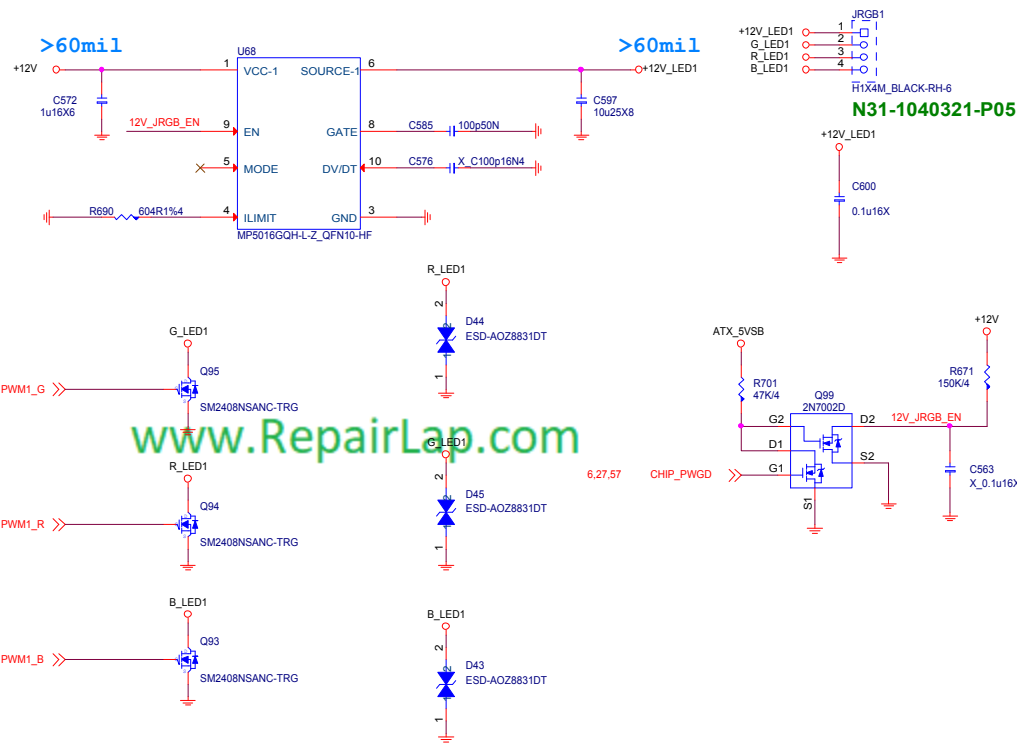


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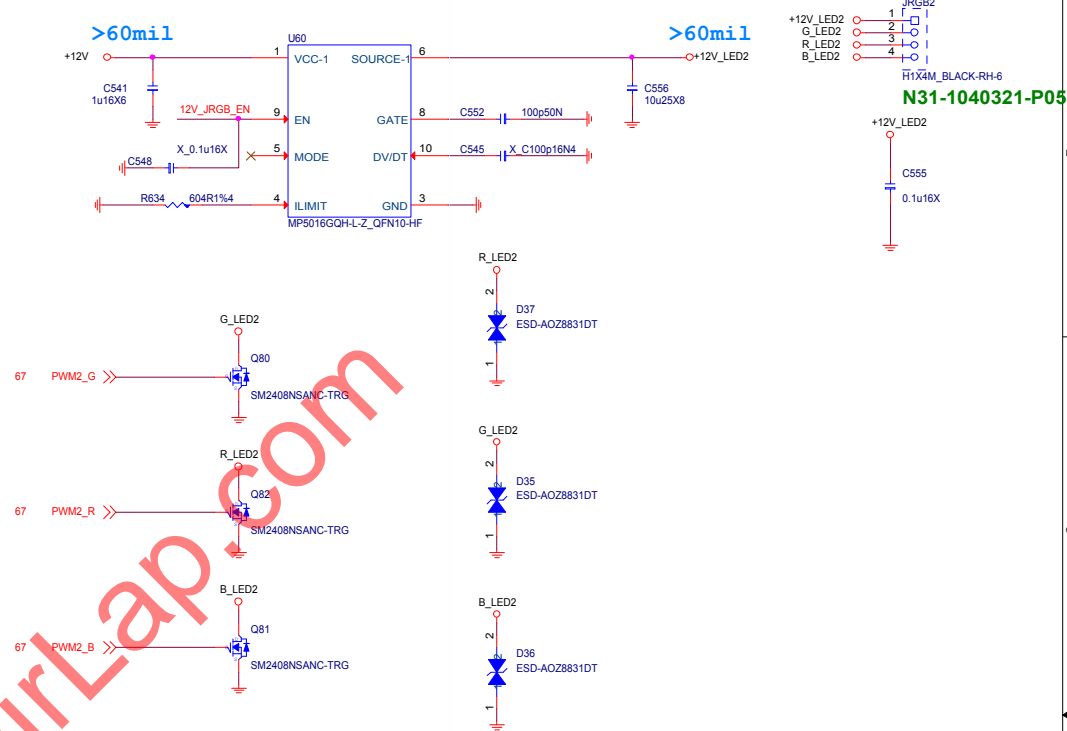
MS-7C91

Size	Document Description	Rev
Custom	LED - Power / JPIPE	10
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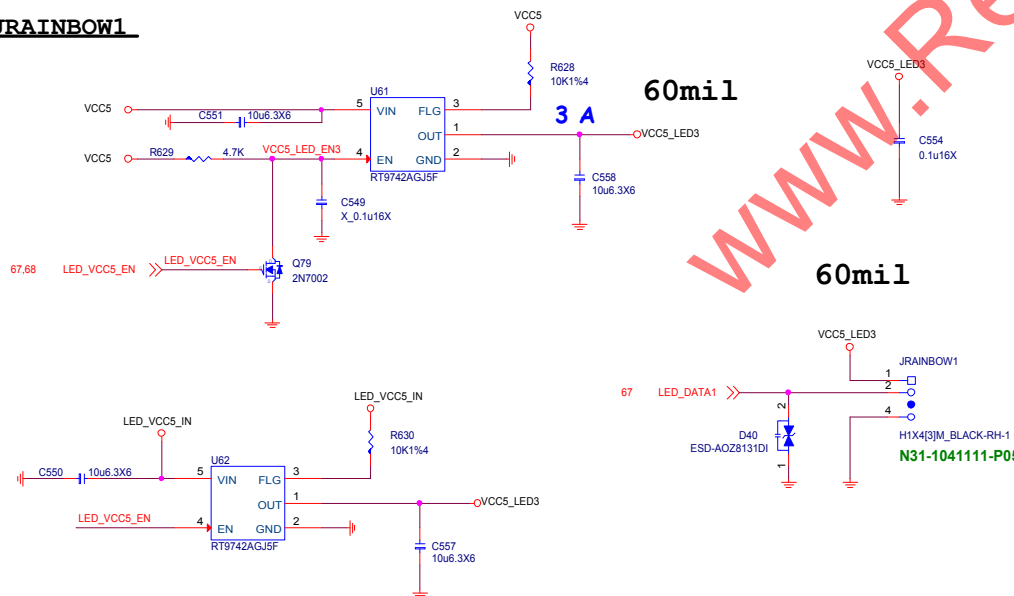
JRGB1



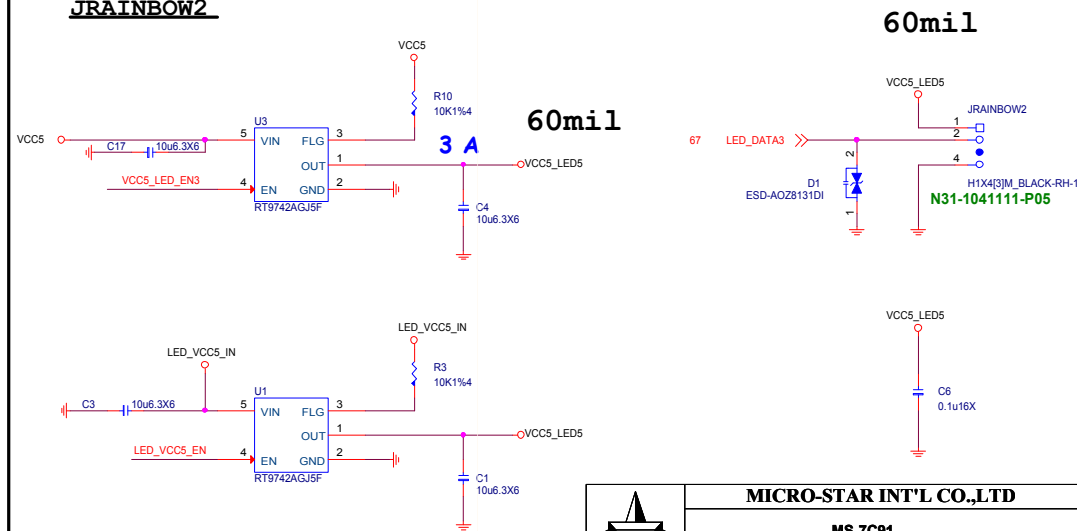
JRGB2



JRAINBOW1



JRAINBOW2

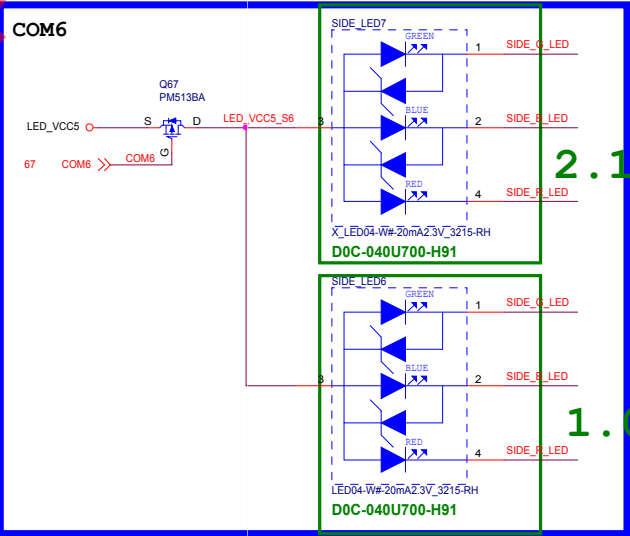
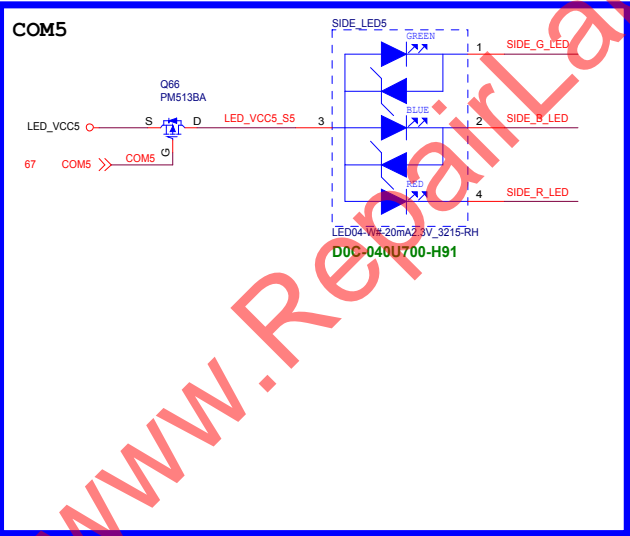
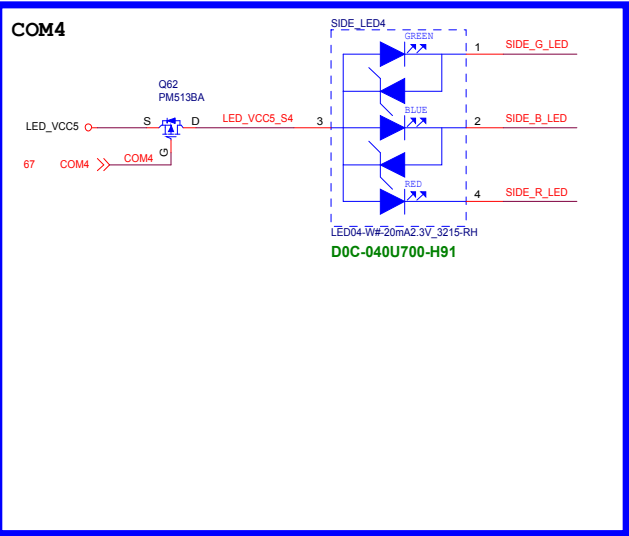
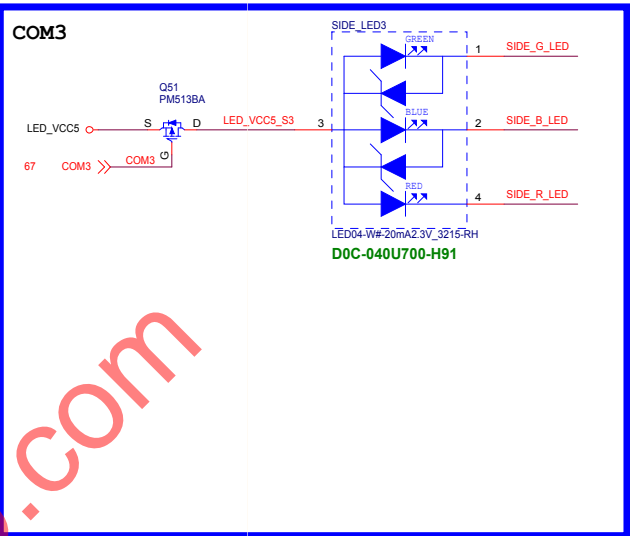
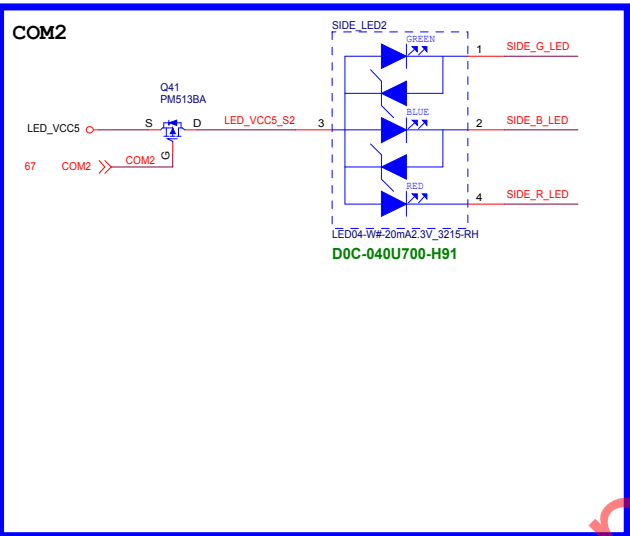
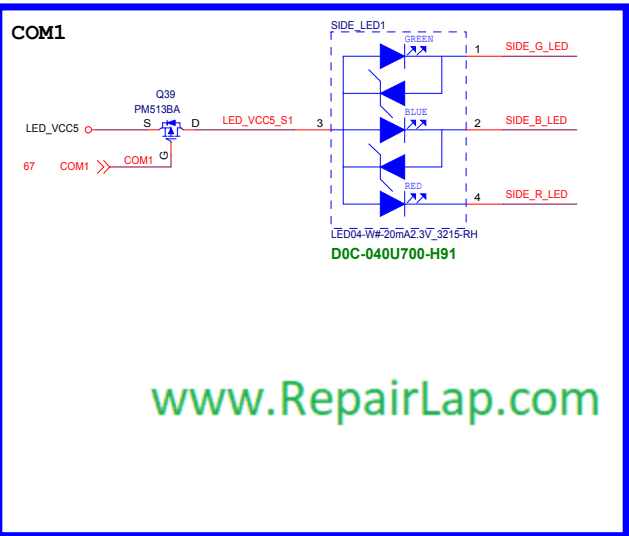


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MS-7C91

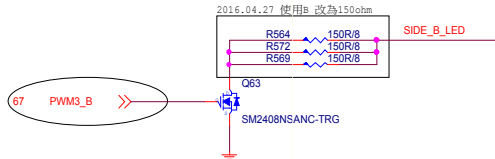
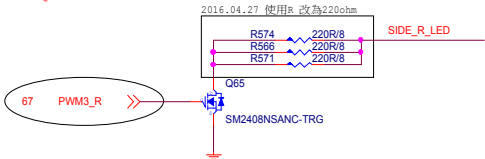
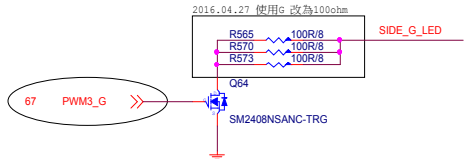
Size	Document Description	Rev
Custom	LED - JRGB1/2_JRAINBOW1/2	10
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BOARD SIDE LED *6




2.1 BOM

1.0 BOM

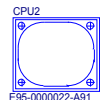


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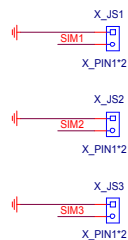
			MICRO-STAR INT'L CO.,LTD		
			MS-7C91		
Size	Document Description				Rev
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CPU Socket

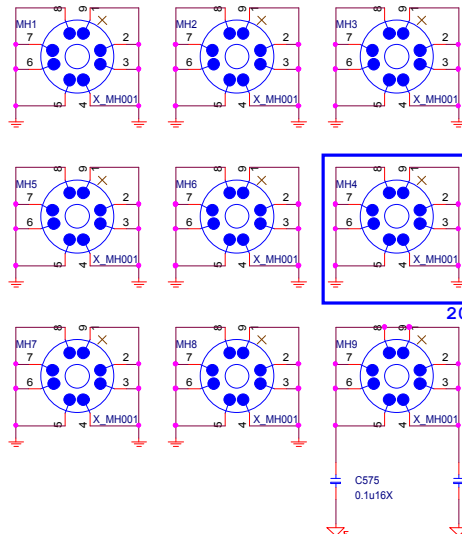


E95-000022-A91

Simulation



Optics Orientation Holes



MANUAL PART

AMI_LAB1
G51-M1SPXXA-A09
G51-M1SPXXA-A09

CFOS1
Y02-MU00170-CFO
Y02-MU00170-CFO

HDMI_LA1
Label
HDMI1
HDMI LABEL
Y01-RHDMI03-000

MKT_LA1
Label
MKT_LABEL
X_MKT LABEL
G51-M1SPP78-Q13

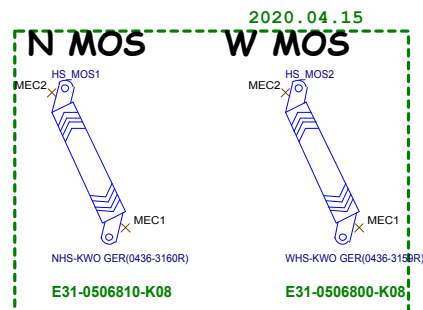
PCB

PCB

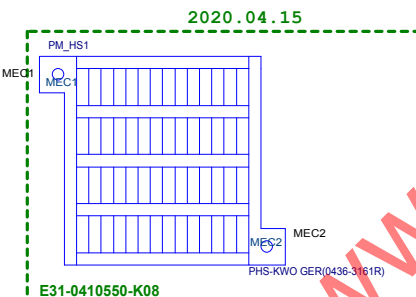


PD0-07C9121-E48
PD0-07C9121-G37

MOS HEATSINK



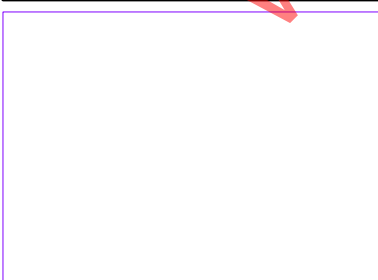
PCH HEATSINK



M2 COVER

IO BRACKET

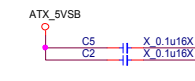
DDR COVER



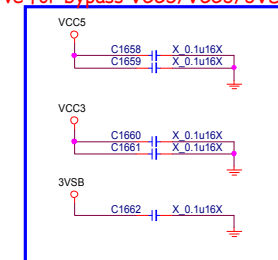
20190201 Remove DDR_COVER1

Moat CAP

Reserve for bypass 12VIN noise use



Reserve for bypass VCC5/VCC3/3VSB noise use



2020.04.14